ARMY
NAVY
AIR FORCE

TM 11-7010-201-40-1
ET821-AA-MMI-01 0/E154 MTS
T 0 31S5-2TSQ73-2-1

TECHNICAL MANUAL

GENERAL SUPPORT MAINTENANCE MANUAL FOR TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT TS-3317( )/TSQ-73 (NSN 1430-01-033-1078) INCLUDING OPERATION AND MAINTENANCE MTS TEST AID ASSEMBLY PART NUMBER TE113980

DEPARTMENTS OF THE ARMY, NAVY, AND AIR FORCE

30 MARCH 1983

WARNING

DANGEROUS VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions.

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas. Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.

Do not be misled by the term "low voltage." Potentials as low as 50 volts may cause death under adverse conditions.

WARNING

Ensure prime power is off to prevent shock hazard to personnel.

WARNING

USE OF CLEANING SOLVENT

Fumes of TRICHLOROTRIFLUOROETHANE are poisonous. Provide adequate ventilation whenever you use 'TRICHLOROTRIFLUOROETHANE. Do not use solvent near heat or open flame. TRICHLOROTRIFLUOROETHANE will not burn, but heat changes the gas into poisonous, irritating fumes. DO NOT breathe the fumes or vapors. TRICHLOROTRIFLUOROETHANE dissolves natural skin oils. DO NOT get the solvent on your skin. Use gloves, sleeves and an apron which the solvent cannot penetrate. If the solvent is taken internally, see a doctor immediately.

WARNING

When extending the MTS, always provide support for both the MTS and the case. Extension of the MTS causes an unbalanced condition and the assembly may tip forward causing personnel ir4ury and equipment damage. WARNING

WARNING

Two men are required to remove the wired plug-in unit test assembly from the case to prevent injury to personnel or damage to the equipment.

LIST OF EFFECTIVE PAGES **INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.**

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TECHNICAL MANUAL
NO. 11-7010-201-40-1
TECHNICAL MANUAL
ET821-M-MMI-010/E154 MTS
TECHNICAL ORDER
TO 31S5-2TSQ73-2-1

DEPARTMENTS OF THE ARMY
THE NAVY, AND
THE AIR FORCE

Washington, DC, 30 March 1983

GENERAL SUPPORT
MAINTENANCE MANUAL
FOR
TEST SET, ELECTRONIC CIRCUIT PLUG-IN UNIT
TS-3317( )/TSQ-73
(NSN 1430-01-033-1078)
INCLUDING
OPERATION AND MAINTENANCE
MTS TEST AID ASSEMBLY
PART NUMBER TE113980

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms), or DA Form 2028-2 located in back of this manual direct to: Commander, US Army Communications-Electronics Command and Fort Monmouth, ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703.

For Air Force, submit AFTO Form 22 (Technical Order System Publication Improvement Report and Reply) in accordance with paragraph 6-5, Section VI, T.O. 00-5-1. Forward direct to prime ALC/MST.

For Navy, mail comments to the Commander, Naval Electronics Systems Command, ATTN: ELEX 8122, Washington, DC 20360.

In either case, a reply will be furnished direct to you.

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VOLUME 2. *TM 11-7010-201-40-2*
Probe Assembly, Test Set - Wire List;
String and Connector (WL10281447)
Test Assembly, Plug-In Unit, Wired, Wire List;
String (WL10281449)
Card Rack Assembly - Analog, Wire List;
String and Connector (WL10281453)

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CHAPTER 1

INTRODUCTION

Section I. GENERAL

1 -1. Scope. This manual contains general support maintenance instructions for Electronic Circuit Plug-In Unit Test Set TS-3317( )/TSQ-73 (figure 1-1). The electronic circuit plug-in unit test set is used with Automatic Telephone Central Office AN/TTC-39 and Automatic Message Switching Central AN/TYC-39. The manual is divided into five volumes. Volume 1 contains three chapters. Chapter 1 is an introduction to the manual. Chapter 2 contains a functional description of the equipment. Chapter 3 provides general support maintenance instructions. Appendix A is a list of reference documents. A glossary is included at the back of volume 1. Volumes 2, 3 and 4 contain wire lists. The electronic circuit plug-in unit test set is hereinafter referred to as the module test set (MTS). Volume 5 contains the MTS test aid for use with the MTS.

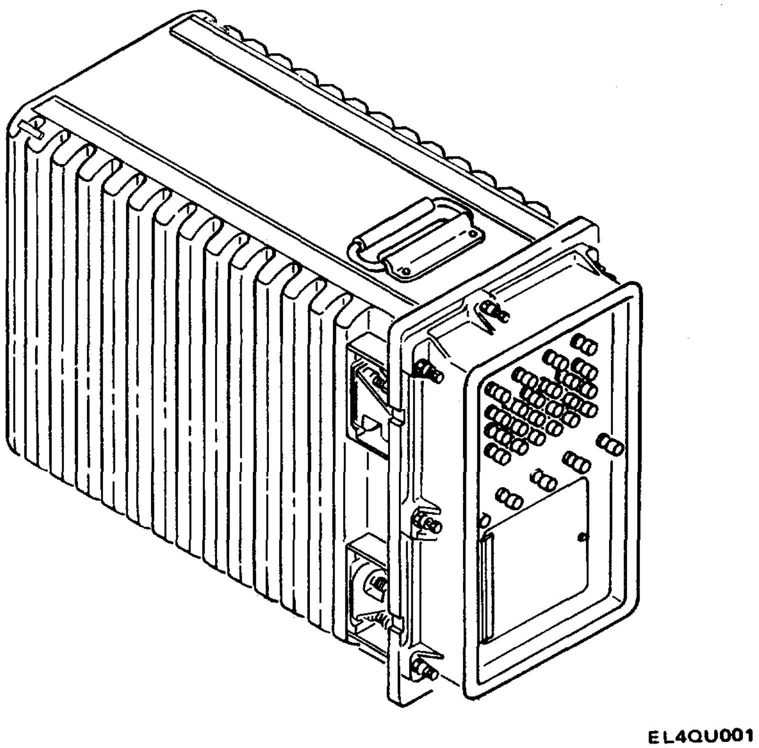


Figure 1-1. Electronic Circuit Plug-In Unit Test Set TS-3317 ( )/TSQ-73

1-2. Consolidated Index of Publications and Blank Forms.

a. *Army.* Refer to the latest issue of DA Pam 310-1 to determine whether there are new editions, changes or additional publications pertaining to the equipment.

b. *Air Force.* Use T.O. 0-1-31 Series Numerical Index and Requirements Table (NIRT).

1-3. Maintenance Forms, Records and Reports

a. *Reports of Maintenance and Unsatisfactory Equipment*. Department of the Army forms and procedures used for equipment maintenance will be those prescribed by TM 38-750, the Army Maintenance Management System. Air Force personnel will use AFR 66-1 for maintenance reporting and TO-00-35D54 for unsatisfactory equipment reporting. Navy personnel will report maintenance performed utilizing the Maintenance Data Collection Subsystem (MDCS) IAW OPNAVINST 4790.2, Vol 3 and unsatisfactory material conditions (UR submissions) IAW OPNAVINST 4790.2, Vol 2, Chapter 17.

b. *Report of Packaging and Handling Deficiencies*. Fill out and forward SF 364 (Report of Discrepancy (ROD)) as prescribed in AR 735-11-2/DLAR 4140.55/NAVMATINST 4355.73/AFR 400-54/MCO 4430.3E.

c. *Discrepancy in Shipment Report (DISREP) (SF 361).* Fill out and forward Discrepancy in Shipment Report (DISREP) (SF 361) as prescribed in AR 55-38/NAVSUPINST 4610.33B/AFR 75-18/MCO P4610.19C and DLAR 4500.15.

1-4. Reporting Equipment Improvement Recommendations (EIR)

a. *Army*. If your Module Test Set needs improvement, let us know. Send us an EIR. You, the user, are the only one who can tell us what you don't like about your equipment. Let us know why you don't like the design. Put it on an SF 368 (Quality Deficiency Report). Mail it to Commander, US Army Communications-Electronics Command and Fort Monmouth. ATTN: DRSEL-ME-MP, Fort Monmouth, New Jersey 07703. We'll send you a reply.

b. *Air Force.* Air Force personnel are encouraged to submit EIRs in accordance with

c. *Navy.* Navy personnel are encouraged to submit EIRs through their local Beneficial Suggestion Program.

1-5. Administrative Storage. Refer to TM 740-90-1, Administrative Storage, for information covering the administrative storage requirements of this equipment.

1-6. Destruction of Army Electronics Materiel. Destruction of Army electronics materiel to prevent enemy use shall be in accordance with TM 750-244-2.

Section II. DESCRIPTION AND DATA

1-7. Description. For a general description and illustrations of the MTS, refer to TM 11-7010-201-12.

1-8. Tabulated Data. For a list of leading particulars and other tabulated data for the MTS, refer to TM 11-7010-201-12.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. OVERALL FUNCTIONAL DESCRIPTION

2-1. Introduction. This chapter provides a functional description of the Module Test Set (MTS). The functional description is presented in two levels: an overall functional description, and a detailed functional description. Section I provides an overall description of how the MTS performs a card test, and covers the following topics: test sequence initiation, continuity tests, functional tests, test sequence completion, and self-test operation. A block diagram of the MTS is shown in figure 2-1.

2-2. Test Sequence Initiation. To perform circuit card identification, continuity tests, and functional tests, the MTS compares data stored in its memory circuits with the outputs of the card under test (CUT). If the card data matches the stored memory data, a passed card test (go condition) is indicated. If a mismatch in data occurs, a failed card test (no-go condition) is indicated. During a card test, the MTS follows a set sequence of operations. This test sequence is started by connecting the test set probe assembly to the card to be tested. A set of six card identification signals (card ID) is applied by the probe function (see figure 2-1) to the timing and control function. There, the card ID is converted to a seven-digit binary code. This binary code identifies the CUT to the MTS and starts the sequence timing. The test sequence is a combination of manual and automatic operations. These operations are explained in the following paragraphs and flow charts. Table 2-1 illustrates flow chart symbology usage. Figure 2-2 is a flow chart showing how the MTS advances step-by-step through a test sequence to accomplish card testing.

2-3. Continuity Test. Continuity testing of circuit cards checks for broken wires or pins in CUT signal paths. During this test, the CUT is in the unit under test (UUT), and the UUT power is on. All signal lines on the CUT should be either a logic ONE (high) or ZERO (low). Since all input pins on the CUT are connected to either a logic output or a pull-up resistor, all logic outputs automatically assume a logic ONE or ZERO state. The MTS applies a 1.5 vdc basis to all signal lines through the test set probe assembly. Each signal line should be greater than 2 vdc (for a logic one) or less than 1 vdc (for a logic ZERO). Any line on the CUT showing less than 2 vdc and more than 1 vdc (i.e., approximately 1.5 vdc) is identified by the error detect logic as a continuity failure. Continuity test errors are displayed on the MTS front panel according to which integrated circuit (IC) on the CUT has the continuity error. Each CONTINUITY ERROR indicator identifies a group of lines in which the malfunction occurred. Each indicator represents 12 lines for cards having six ICs, or 14 lines for cards having five ICs. The CONTINUITY ERROR indicators (left to right) correspond to the ICs (top to bottom) on the CUT. Further isolation of the continuity error requires probing of connector J7 on the MTS front panel. Some cards in the system have ICs with unused pins. Since these pins have no connection on the card or inside an IC, the associated IC would normally fail any continuity test. However, the generated card ID is applied to a mask function (see figure 2-1). The mask function generated an input/output (I/O) pin mask. The pin mask allows the unused pins to pass the continuity test.

2-4. Functional Test. The functional test consists of a truth table verification of the Card Under Test (CUT). A truth table for each type of IC in the system is stored in the control memory function (see figure 2-1). The control memory test data (test pattern) is applied by the probe function to the CUT. Return data from the CUT is passed by the probe function and applied to the error detect function. The error detect function compares the return data from the CUT with the truth table (compare data),stored in data memory. The appropriate FUNCTIONAL INPUT ERROR and FUNCTIONAL OUTPUT ERROR indicators on the MTS front panel signify the results. The indicators (left to right) correspond to ICs (top to bottom) of the CUT. The functional test is performed on one IC at a time, except for the 587117 card. On this card, all ICs are tested at the same time. The mask and control memory functions, which control test length and any special clocking, are enabled by the timing and control function. The mask data output disables all probe function output gates except those related to the specific IC under test. The mask data is identified by a function of the card ID from timing and control.

2-5. Test Sequence Completion. Upon completion of the continuity and functional tests, the timing and control function (see figure 2-1) returns the MTS to its original idle condition. The front panel GO or NO-GO indicator remains lighted, depending on successful or unsuccessful completion of the tests. If a test sequence is to be repeated, either the test set probe assembly is removed and reattached to the CUT, or the REPEAT CYCLE switch is pressed and released. If continuous testing is required, the CONTINUOUS CYCLE switch is pressed and released. The CONTINUOUS CYCLE indicator should be on for continuous operation and off for single-cycle operation.

2-6. Self-Test Operation. Self-test is started by attaching the test set probe assembly to terminal board TB101 (self-test strip) located behind the access door on the front panel. A self-test card ID is generated by the probe function, and is applied to the self-test function (see figure 2-1) through the probe function. The self-test function generates dummy card ID signals corresponding to the card ID signals of the MTS testable system cards. One at a time, the dummy binary-coded card IDs are applied to the data memory and mask functions. The MTS performs the card test sequence for each card, with the self-test function supplying the test results. Each card ID test sequence is performed until all possible function testing information is checked. If an error occurs, the MTS continues testing the same function on the dummy card ID where the error is detected. To continue the self-test, the SELF-TEST switch on the front panel must be pressed and released. If no error is detected, the MTS has passed the self-test and is in proper working condition. The MTS requires approximately 7 seconds to complete the self-test sequence (without error).

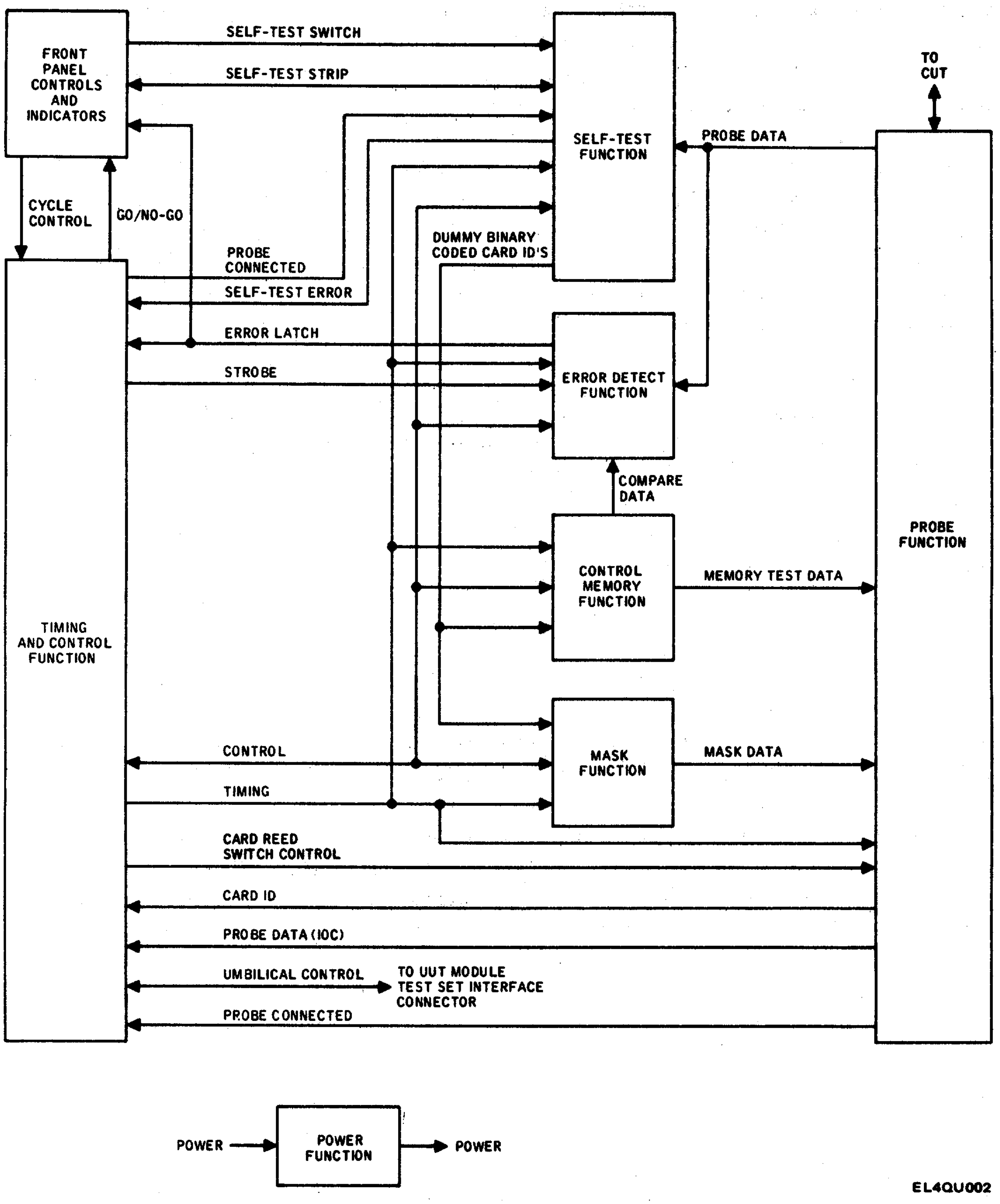
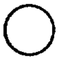
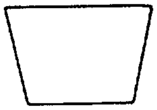
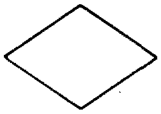
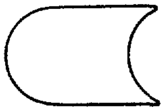
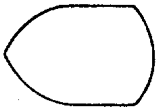
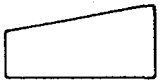
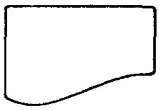
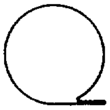
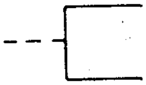
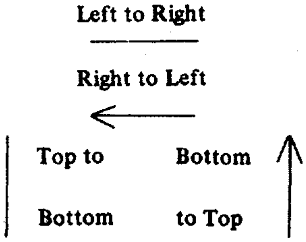
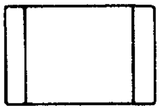


Figure 2-1. Module Test Set Block Diagram

Table 2-1. Flow Chart Symbology

	Terminal Symbol-represents a terminal point in the flow chart such as start, stop, halt, delay, or interrupt. Data may enter or leave at this point.
	Connector Symbol - represents a junction in a line of flow. A set of two is used to represent a continued flow direction when the flow is broken by chart limitations.
	Manual Operation Symbol-represents any off-line function or process geared to human speed.
	Decision Symbol-represents a decision on switching type operation that determines which of a number of paths is to be followed.
	On-Line Storage Symbol-represents an I/O function utilizing mass information storage that can be accessed on-line.
	Display Symbol-represents an I/O function in which the information is displayed for human use at the time of processing (i.e., indicators, printouts ,plots, etc.).
	Manual Input Symbol-represents an I/O function in which information is manually entered through on-line keyboards, switch settings, card readers, push buttons, etc.
	Document Symbol-represents an I/O function in which the medium is a document.
	Magnetic Tape Symbol -represents an I/O function in which the medium is magnetic tape.
	Annotation Symbol-represents the addition of descriptive comments or explanatory notes. A broken line may be drawn to the left or to the right and connected to the flow line at its most meaningful point.
	Process Symbol-represents the processing functions in which the process of executing a defined operation or group of operations results in a change in value, form, or location of information.
	Flow Line Symbols-represent the direction of information or operational flow.
	Predefined Process Symbol-represents a named process consisting of one or more operations or program steps specified elsewhere (not this flow chart).

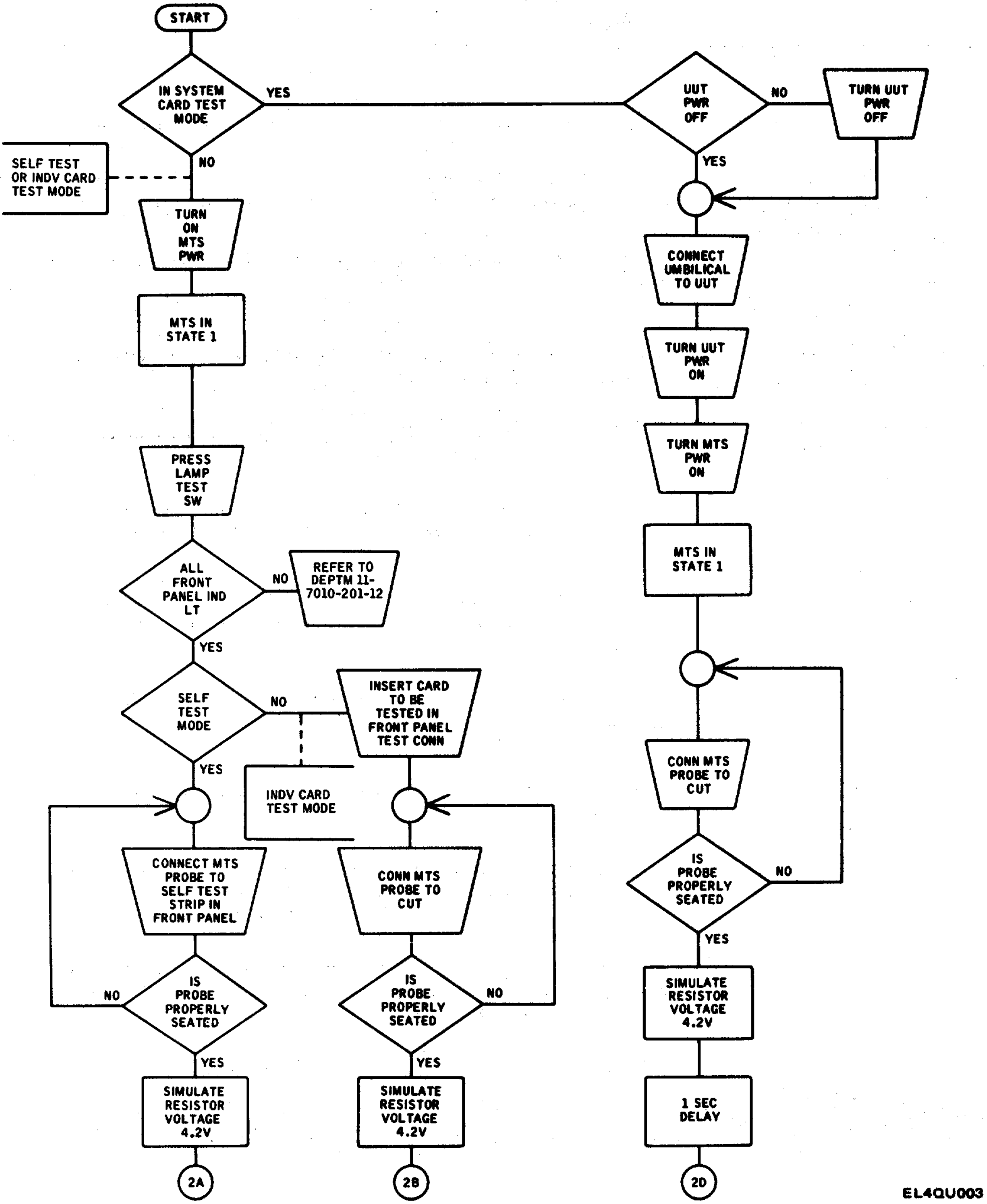


Figure 2-2. Test Sequence Flow Chart (Sheet 1 of 7)

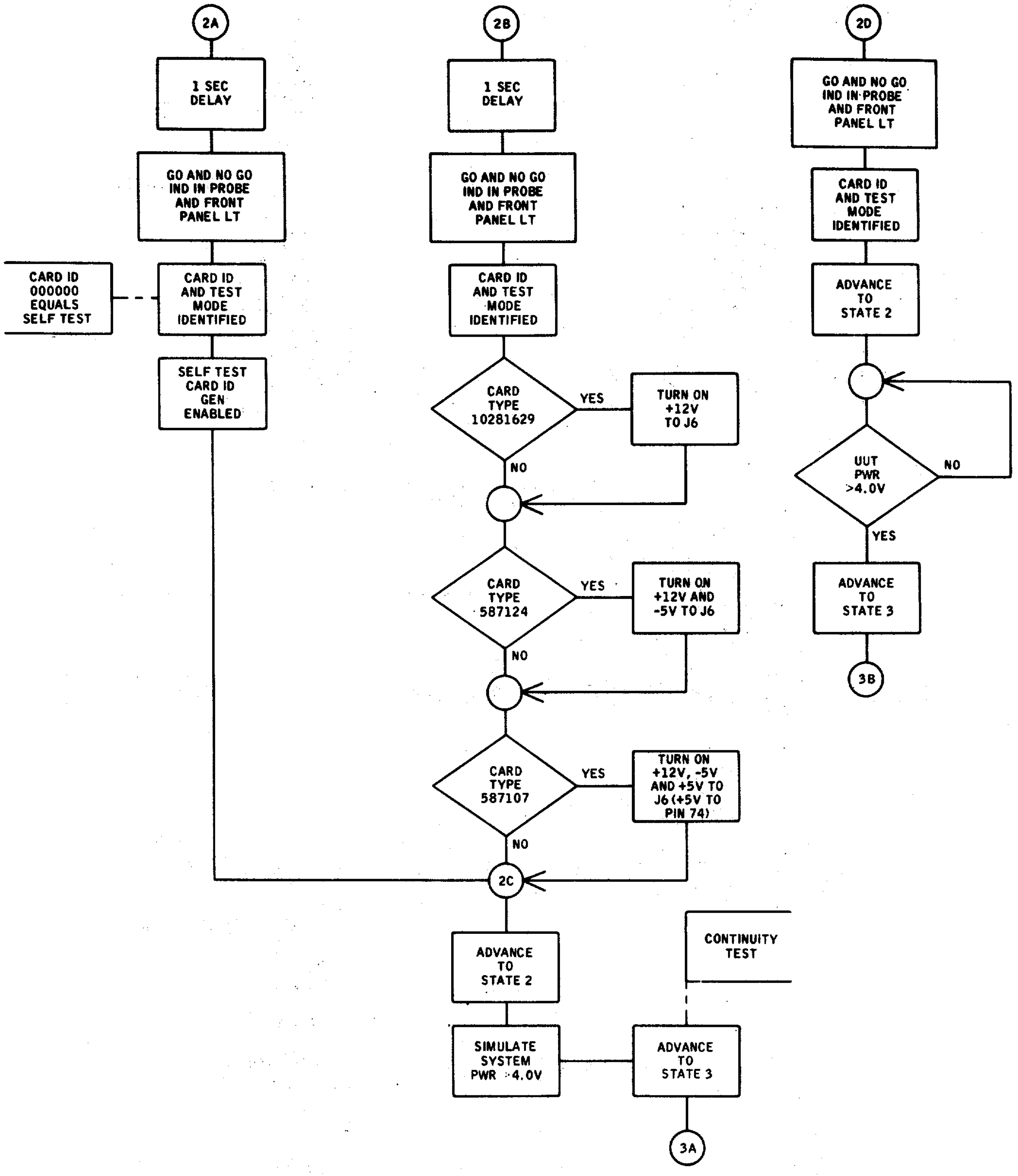


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Figure 2-2. Test Sequence Flow Chart (Sheet 2 of 7)

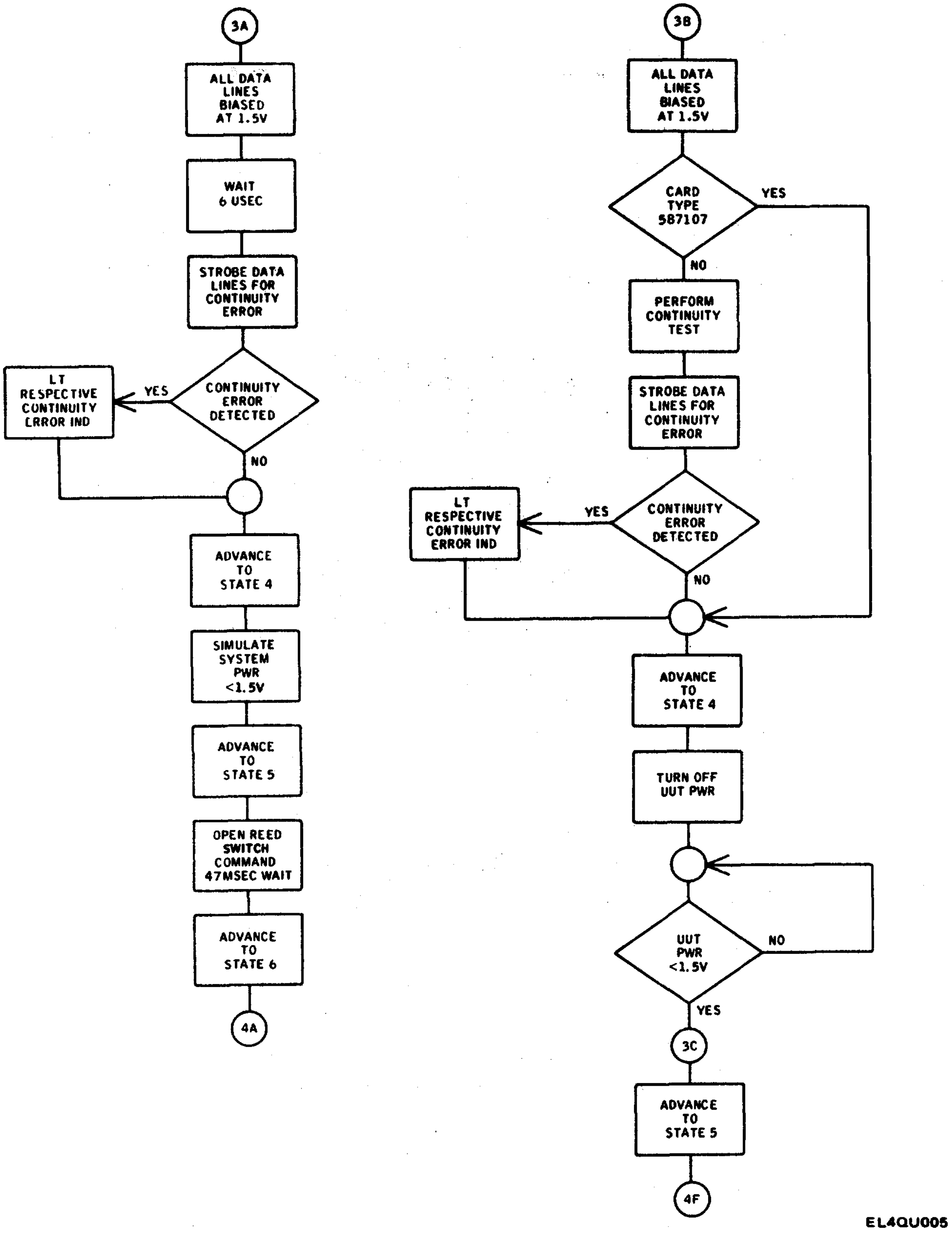

Figure 2-2. Test Sequence Flow Chart (Sheet 3 of 7)

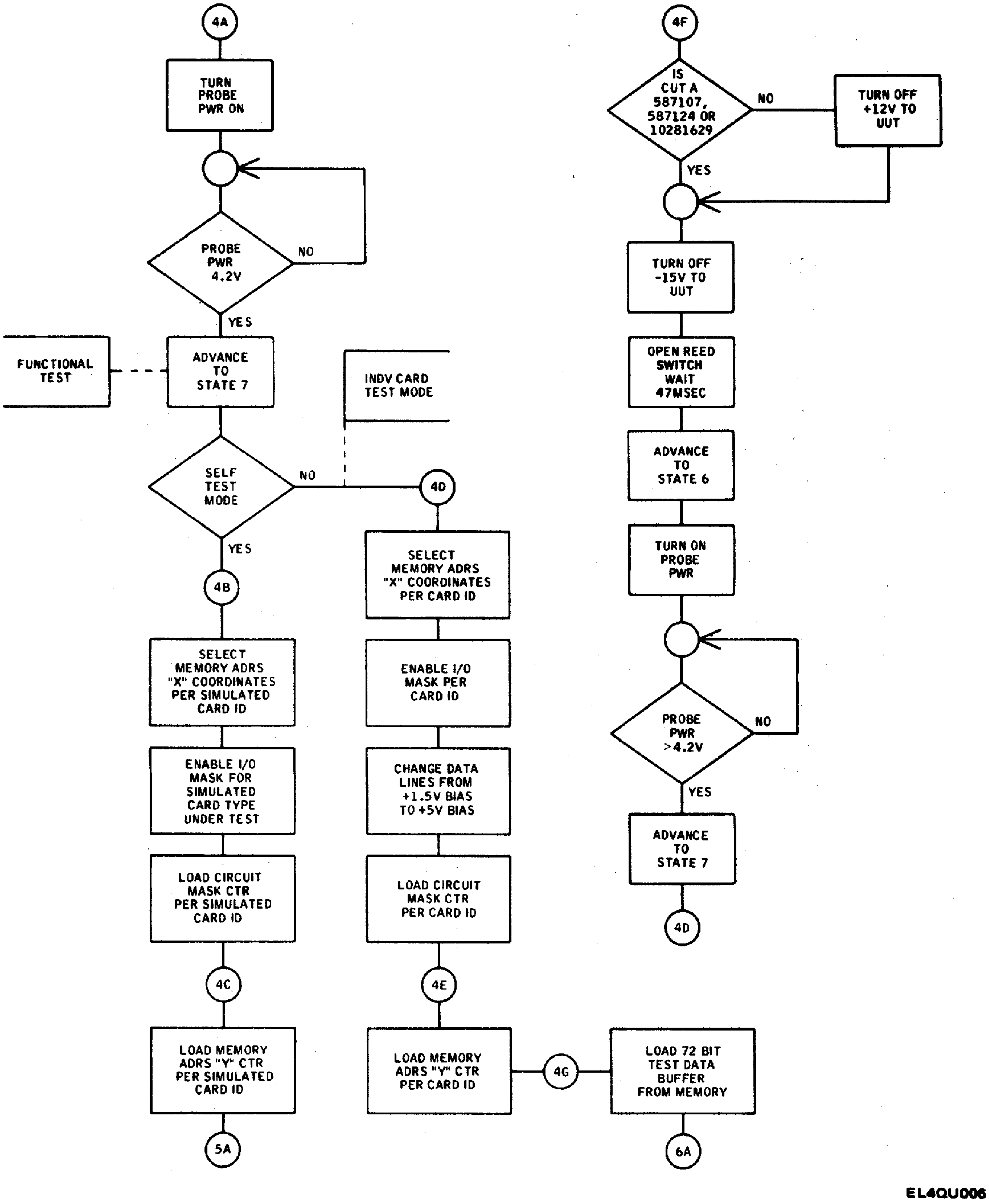

Figure 2-2. Test Sequence Flow Chart (Sheet 4 of 7)

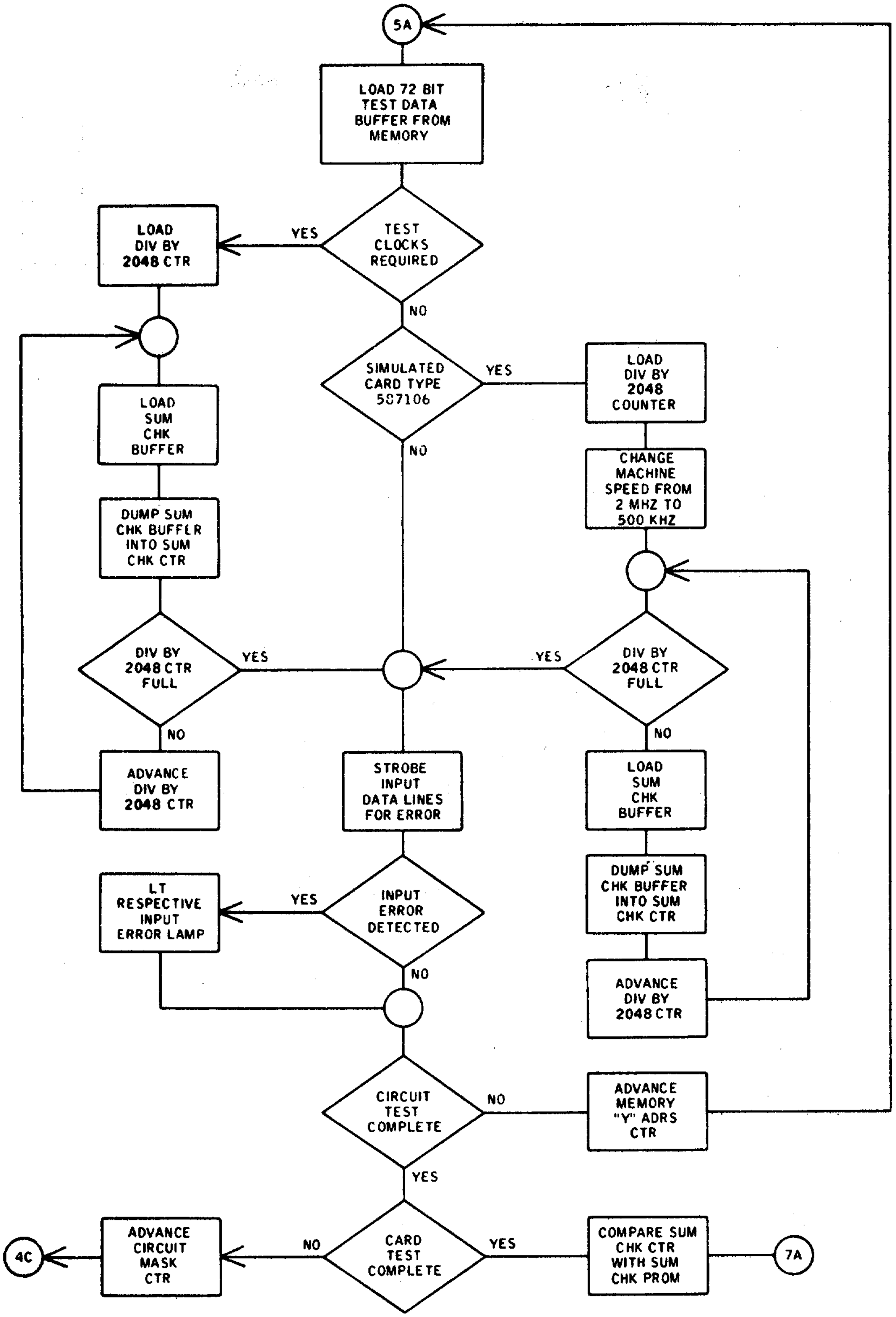

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Figure 2-2. Test Sequence Flow Chart (Sheet 5 of 7)

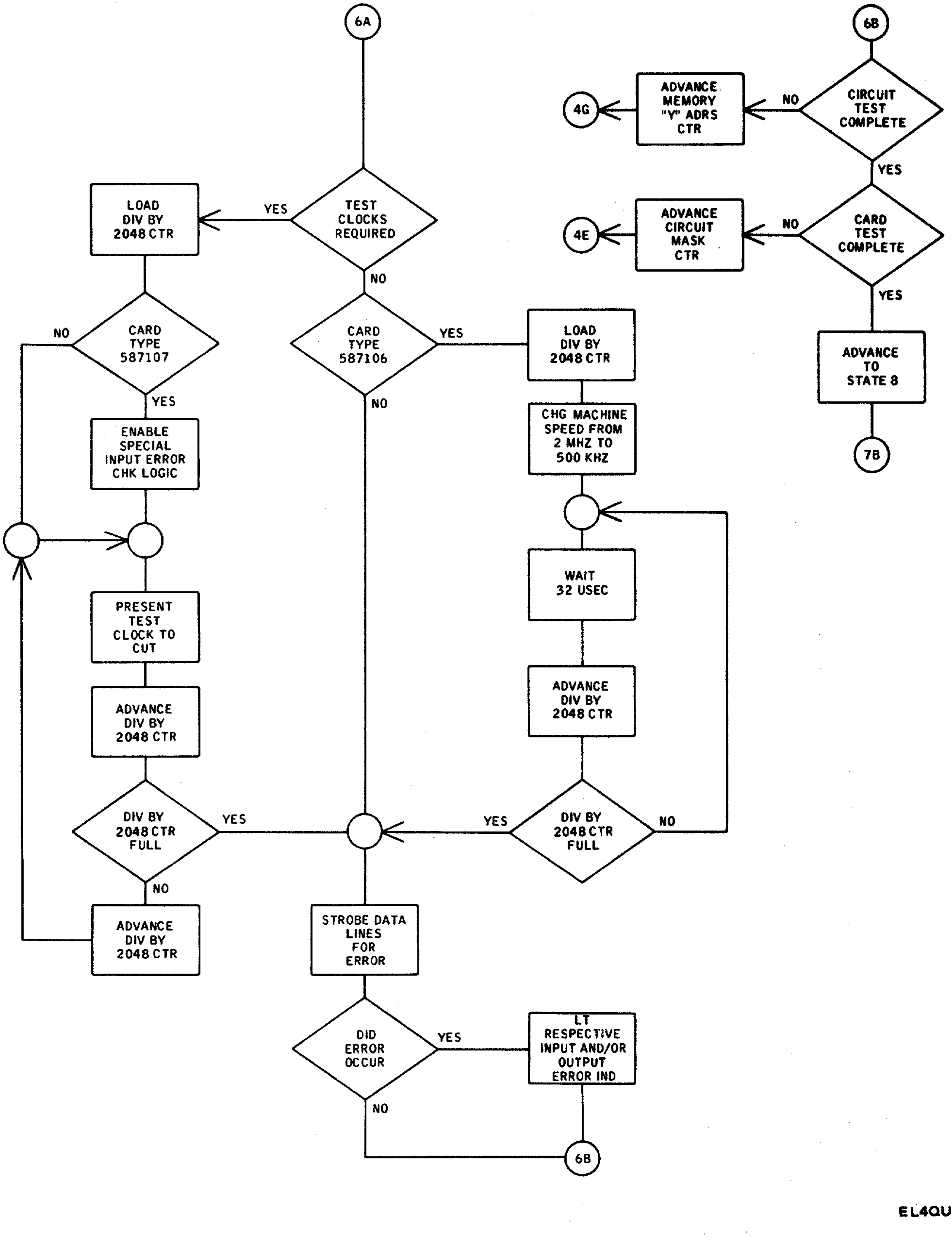


Figure 2-2. Test Sequence Flow Chart (Sheet 6 of 7)

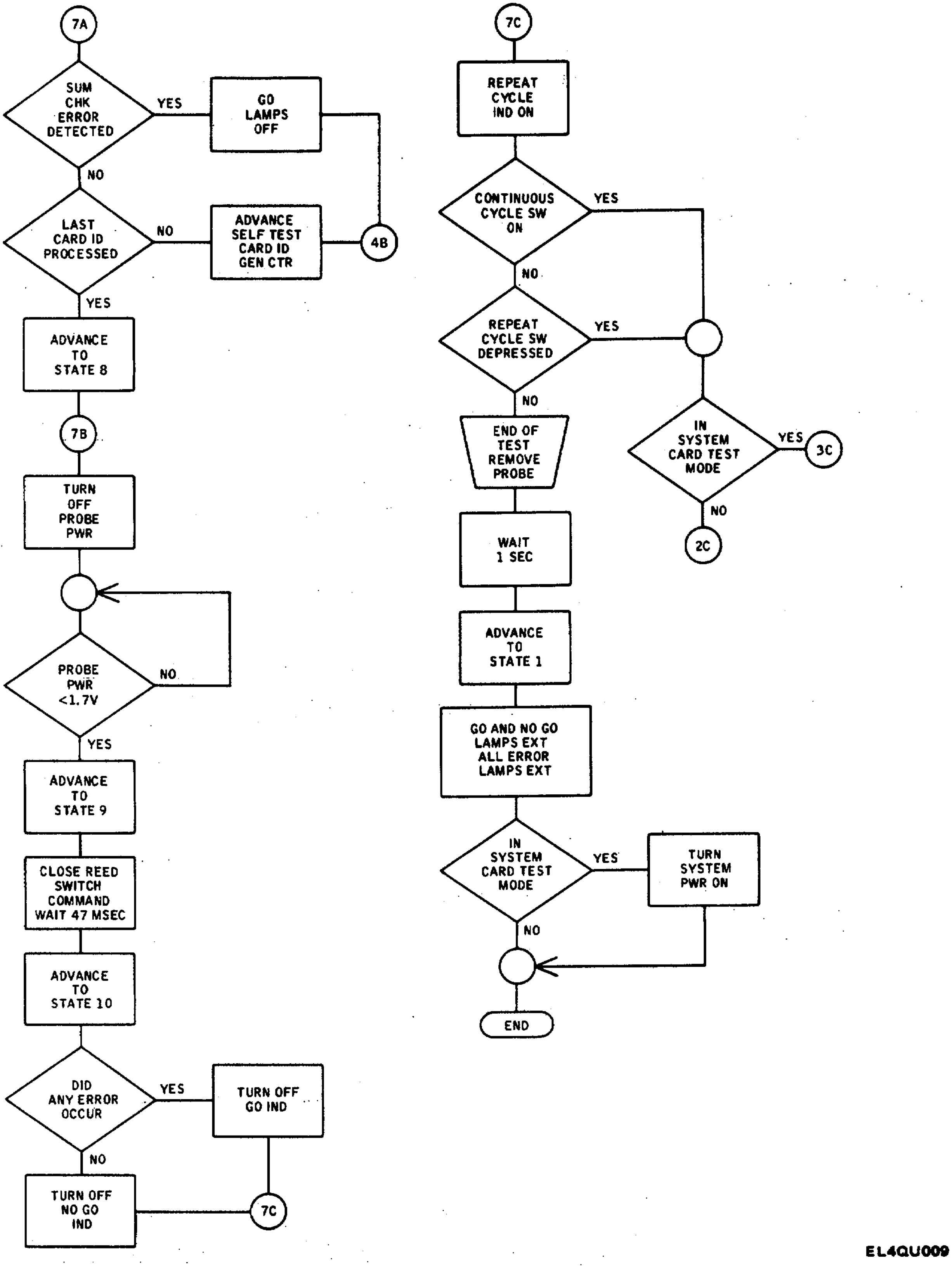


Figure 2-2. Test Sequence Flow Chart (Sheet 7 of 7)

Section II. DETAILED FUNCTIONAL DESCRIPTION

2-7. Introduction. This section provides a detailed functional description of the MTS. The following functions are described: timing and control, mask, control memory, error detect, self-test, probe, and power. Block diagrams support the functional descriptions. Operation of each function is described for an in system card test. When an individual card test is performed, the MTS simulates the UUT function.

2-8. Timing and Control Function. The timing and control function (see FO-2 in back of manual) operates sequentially in 10 states, under control of a state generator. State generator sequencing is shown in figure 2-3. The following paragraphs .describe the 10 states of the state generator.

a. *State 1*. State 1 is the idle condition for the timing and control function. Operation is started BY attaching the test set probe assembly to the CUT. The card ID of the CUT is automatically generated BY the probe function and applied to the card ID decoder logic. This starts the action of a 1-second delay one shot. The I-second delay ensures proper probe assembly connection to the CUT. The random card ID signal, generated by the card ID decoder logic, is applied to the self-test function and to the card ID random to-binary logic. This results in a binary-coded, seven-digit card ID. After the I-second delay, the output of the one-shot advances the state generator to state 2.

b. *State 2.* The state 2 signal (probe connected) is applied to the card ID random-to-binary logic. This signal enables the binary-coded card ID to all involved MTS circuits. During self-test, the probe-connected signal is applied to the self-test function. The logic control tests the UUT for a power-on condition (greater than 4.0 vdc). If UUT power is on, the state advance signal from the logic control enables state 3.

c. *State 3.* The state 3 signal (perform continuity test) is applied to the continuity strobe generator logic. The resulting strobe signal is applied to the error detect function. After the strobe is generated, a. continuity test complete signal is applied to the state generator. The test complete signal enables state 4.

d. *State 4.* The state 4 command (turn off UUT power) causes the logic control to turn off UUT power. When the logic control senses that UUT power is off (less than 1.5 vdc), the state advance signal from the logic control enables state 5.

e. *State 5*. The state 5 command (isolate CUT) causes logic control to isolate the card from the UUT. To isolate the card, the probe function commands the CUT reed switch to open.

NOTE

> Some circuit cards have a reed switch that is controlled by an electromagnet in the probe. Other cards have a reed relay which opens in state 4 when UUT power is turned off. In either case, the purpose of the switch or relay is to disconnect the +5v supply line to the CUT during testing.

The reed switch open signal triggers a 47-millisecond delay one-shot. The delayed one-shot output advances the state generator to state 6 under control of the delayed advance signal.

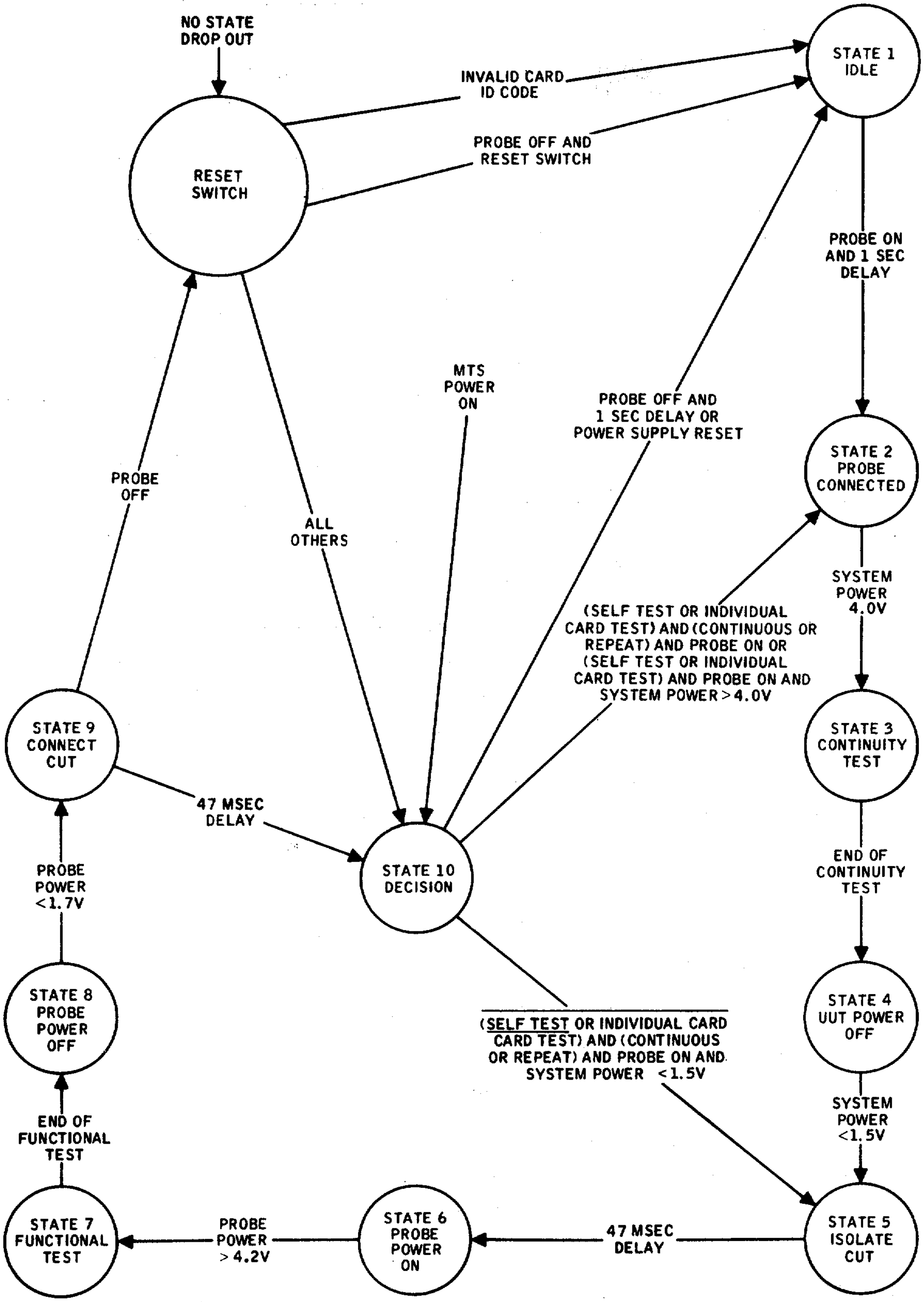


Figure 2-3. State Generator Sequencing

f. *State 6*. The state 6 command (turn on probe power) notifies the logic control to turn on power in the probe function. The logic control senses this condition (greater than 4.2 vdc) and enables state 7 with the state advance signal.

g. *State 7* During state 7, several operations occur to accomplish functional testing of the CUT.

(1) The state 7 pulse is transferred to the functional test timing generator. The functional test timing generator then generates the basic timing signals for the functional test operations.

(2) The state 7 pulse is applied to the control memory function and the mask function. This enables the binary-coded card ID signal (through the control memory and mask functions logic) to identify the card type and circuit to be tested. The mask function then masks off all pins on the card except those applicable to the circuit to be tested.

(3) If the card is an input/output controller (IOC) card, it cannot be checked in the normal manner. In this case, a control memory function output causes the IOC card error detect logic to sense the card type. The IOC card error detect logic checks the CUT output (probe data IOC) for errors.

(4) The IC counter logic receives decoded binary ID information (number of circuits) from the control memory function. The IC counter logic also receives the card type (card group) from the mask function. The IC counter logic advances the mask and control memory functions each time an IC test is complete (IC count). When all ICs on the CUT have been tested, the IC counter logic output enables the control memory function. This returns a card test complete signal to the state generator.

(5 If the CUT requires clock signals for testing, the control memory function enables the test clock generator (card type). One test clock pulse (1-microsecond pulse width) is genemted each MTS cycle. The specific number of total clocks is determined by the control memory function. When that number is reached, the control memory function sends a full count signal to stop the test clock generator.

(6) If an error is detected during the tests, the error lamp logic is enabled by the error latch or IOC error signal. This lights the applicable error indicator.

(7) When the functional tests are completed, the IC counter logic function enables state 8 (card test complete).

h. *State 8.* The state 8 command (turn off probe power) causes the logic control to turn off probe power. When the logic control senses power is off (less than 1.7 vdc) the logic control state advance signal enables state 9.

i. *State 9.* The state 9 command (connect CUT) causes the logic control to reconnect the card to the UUT with the card reed switch control signal. The probe function commands the reed switch to close. The reed switch closed signal triggers a 47-millisecond delay one-shot. The one-shot output advances the state generator to state 10 with the delayed state advance signal.

j. *State 10*. In state 10, testing is either continued for another cycle (CONTINUOUS CYCLE switch on, or REPEAT CYCLE switch activated) or terminated. On receipt of the cycle control signal input, the logic control advances the state counter to the appropriate state.

2-9. **Mask Function**. The mask function (see figure 2-4) consists of the I/O mask, gross card type decoder logic, sliding circuit mask, and unused pin mask. The mask function i8 addressed by the binary coded card ID signal from the timing and control function, or the dummy binary coded card ID from the self-test function. The mask function is activated at state 7 time by the state 7 command (perforn functional test). Internal timing is provided by the functional test timing signal.

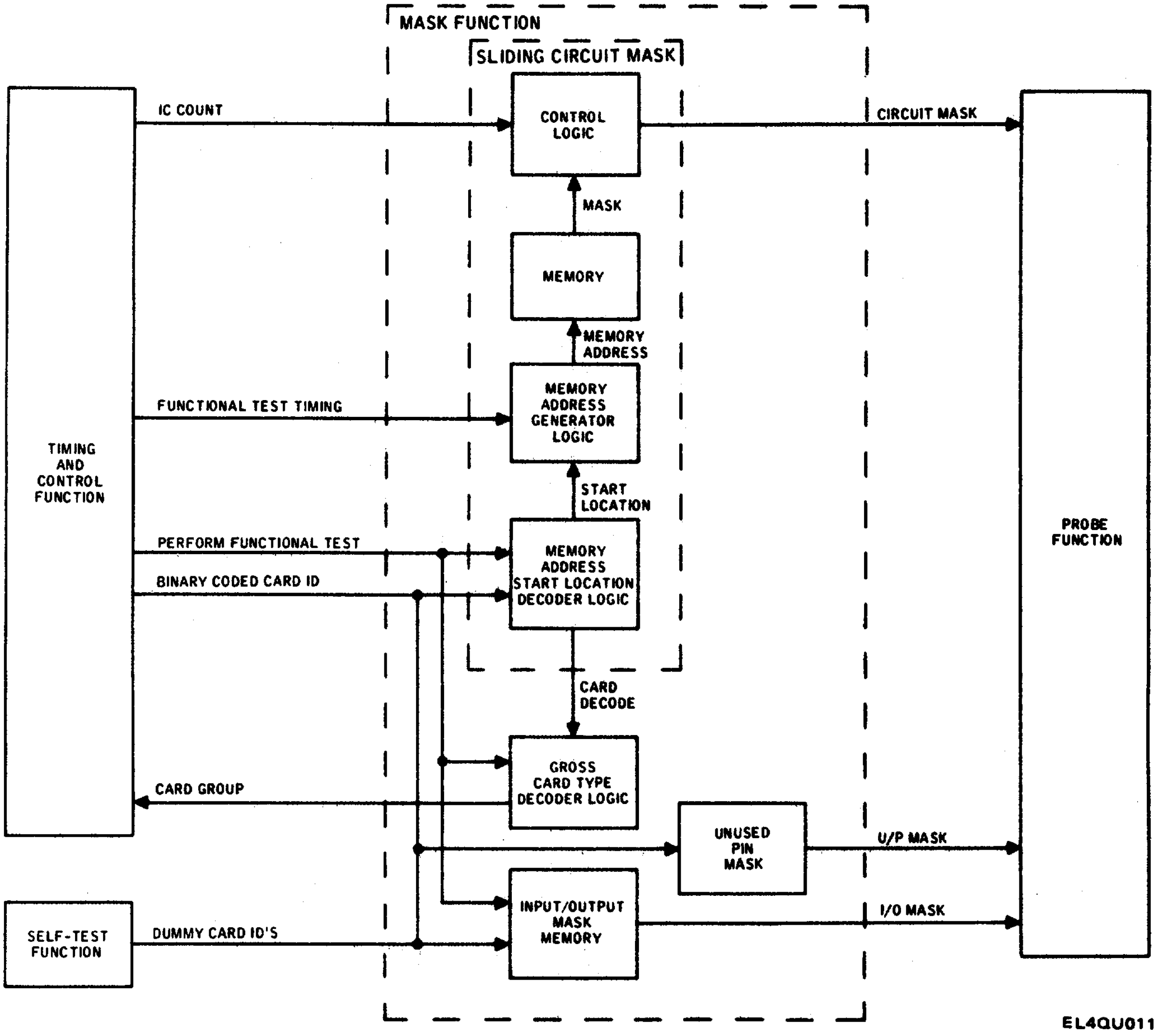


Figure 2-4. Mask Function Block Diagram

a. *IIO Mast* The **I/O** mask determines which probe signal lines are used for input and which are used for output. The I/O mask also controls the probe control logic gates according to the CUT.

b. *Gross Card Type Decoder Logic* The gross card type decoder logic accepts the card decode signal from the memory address start location decoder logic. When enabled by the state 7 command, it generates a card group signal. The timing and control function uses the card group signal to identify the CUT card group. The card groups are as follows:

(1) Card group a: cards with one circuit per card.
(2) Card group b: card with six single-circuit ICs.
(3) Card group c: cards with five single-circuit ICs.
(4) Card group d: cards with six multiple-circuit ICs.

c. *Sliding Circuit Mask* When enabled by an IC count pulse, the sliding circuit mask blocks off pins to all CUT circuits except those pins connected to the circuit to be tested. This is accomplished through the probe function. Pin masking is performed according to the CUT card group.

(1) *Card group a.* When the CUT is in card group a, circuit masking is not required, since the CUT contains only one circuit. The 1/0 mask identifies the required 1/0 pins of the CUT, and the sliding circuit mask is not enabled during a cat d group a test.

(2) *Card group b.* When the CUT is in card group b, circuit masking is required since the card contains more than one IC. The IC count signal from the timing and control function allows the control logic to enable the probe function. The probe function then enables the pins to the first IC of the CUT. When testing of the first IC is complete, the IC count signal is advanced. This steps the control logic to enable the probe function, and the pins of the next IC of the CUT. This process continues until all ICs on the CUT have been tested.

(3) *Card group c.* The procedure for masking cards from card group c is identical to that described for card group b.

(4) Card *group* d. When the CUT is from card group d, more circuit masking is required since each IC on the CUT contains more than one circuit. The IC count signal still allows the control logic to enable the probe function for each IC on the CUT. This is the same action as that described for card group b. To provide a valid test, all circuits within the IC (except the one being tested) must be masked by the memory. The address for the memory is derived from application of the binary-coded card ID to the memory address start location decoder logic. The memory address start location decoder logic generates a start location. This signal is loaded into the memory address generator logic, which directly addresses the memory. The resulting memory mask, when applied to the control logic, enables testing of the first circuit of each IC, and remains constant until each IC has been tested. At this time, the functional test timing signal advances the memory address generator logic by one count. This changes the memory address applied to the memory. The new memory mask corresponds to the next circuit in the ICs, and remains constant until that circuit in each IC is tested. This process continues until all circuits of-all the ICs on the CUT have been tested.

d. *Unused Pin Mast* On receipt of the binary-coded card ID, the unused pin mask determines which pins have no connection on the CUT. These pins are masked from any testing functions.

2-1 0. Control Memory Function. The address logic test pattern of the test pattern memory (X-address, Y-address, Y-address stop) accepts the binary coded card ID from the timing and control function (see figure 2-5). The address test pattern is used as an address to select the correct stored information corresponding to the CUT. The Y-address start signal from the Y-address start location decoder logic (binary 1 to 63) is applied to the Y-address generator logic. This occurs when the Y-address start signal is enabled by the state 7 signal (perform functional test). The Y-address corresponding to the start location number is then generated. This address, along with the Y-address stop signal from the Y-address stop location decoder logic, is applied to the card test complete detect logic. The Y-address generator logic will advance one bit each time a new test pattern bit is used. When its output reaches the same number as the stop location, and after that bit has been error checked, the card test complete logic notifies the timing and control function that the circuit test is complete. The next circuit on the CUT is then enabled (by the timing and control function) and the same test pattern is repeated. The test pattern will continue to repeat until the IC counter logic in the timing and control function generates a card and self-test complete signal. The quantity-of-circuits-per-IC decode logic stores the number of ICs to be tested. This logic also contacts the timing and control function through the number of circuits signal. The card type decode logic determines the card type being tested. It also notifies the test clock generator (with the card type signal) in the timing and control function if clocks are required for that card. The same logic supplies the error detect function with comparison data (compare data) for error checking. At the same time (state 7), the binary X and Y addresses are applied to the test pattern memory logic and the control word memory logic. The test pattern memory logic reads the selected test pattern data to the probe function for application to the CUT. The control word memory logic contains the number of clock pulses required for that functional test pattern. That number is transferred to the test clock counter logic. When the full count is reached, the error detect function makes a comparison of the stored CUT data. The full count signal is then transferred to the test clock generator (timing and control function) to stop the count.

2-11. Error Detect Function. The error detect function (see figure 2-6) is performed by 12 data comparator cards. Each card consists of six comparison channels, two latching lamp drivers, two nonlatching lamp drivers, and a 64-word by eight-bit programmable read-only memory (PROM). The PROM receives a six- bit control address corresponding to the card ID from the card type decode logic. An eight-bit memory word (test control) is generated and applied to the data comparison channels. This enables or inhibits the comparators and assigns data lines to the appropriate front panel indicator. The probe data (up to 72 lines) is compared to the compare data from the control memory function in the data comparison channels. The results (channel output signals) are applied to the latching lamp driver logic. If the channel output is low, the comparison is favorable. If the channel output is high, a potential error condition exists. During state 3, the timing and control function applies a strobe pulse to the latching lamp driver logic. If an error is present, the latch switches. It then enables the corresponding front panel indicator(s) (CONTINUITY ERROR) with the error latch signal. During state 7, the functional test timing signal from the timing and control function is applied to the latching lamp driver logic. If an error is present, the latch is switched. The applicable front panel indicator (FUNCTIONAL INPUT ERROR or FUNCTIONAL OUTPUT ERROR) is lighted.

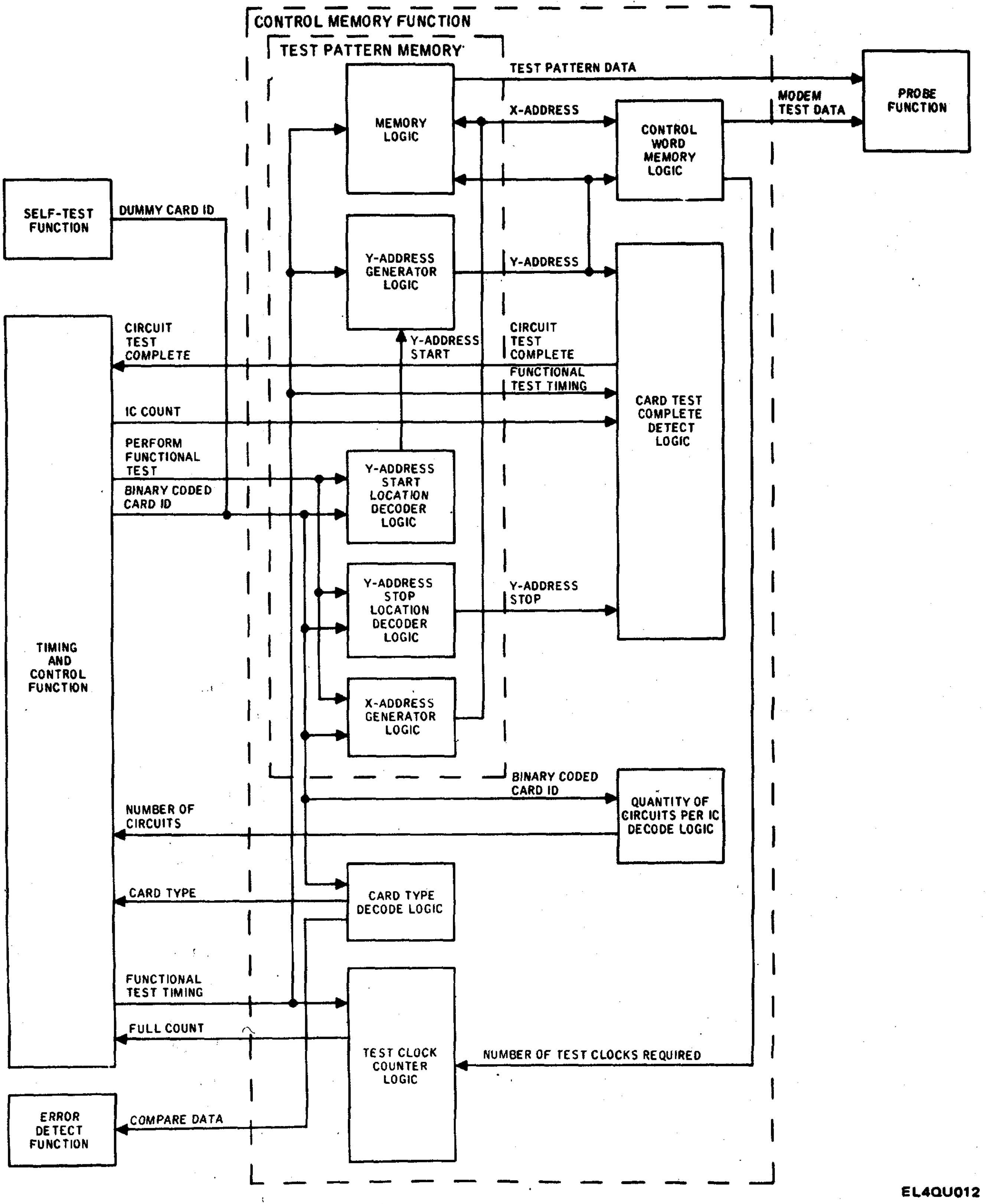


Figure 2-5. Control Memory Functional Block Diagram.

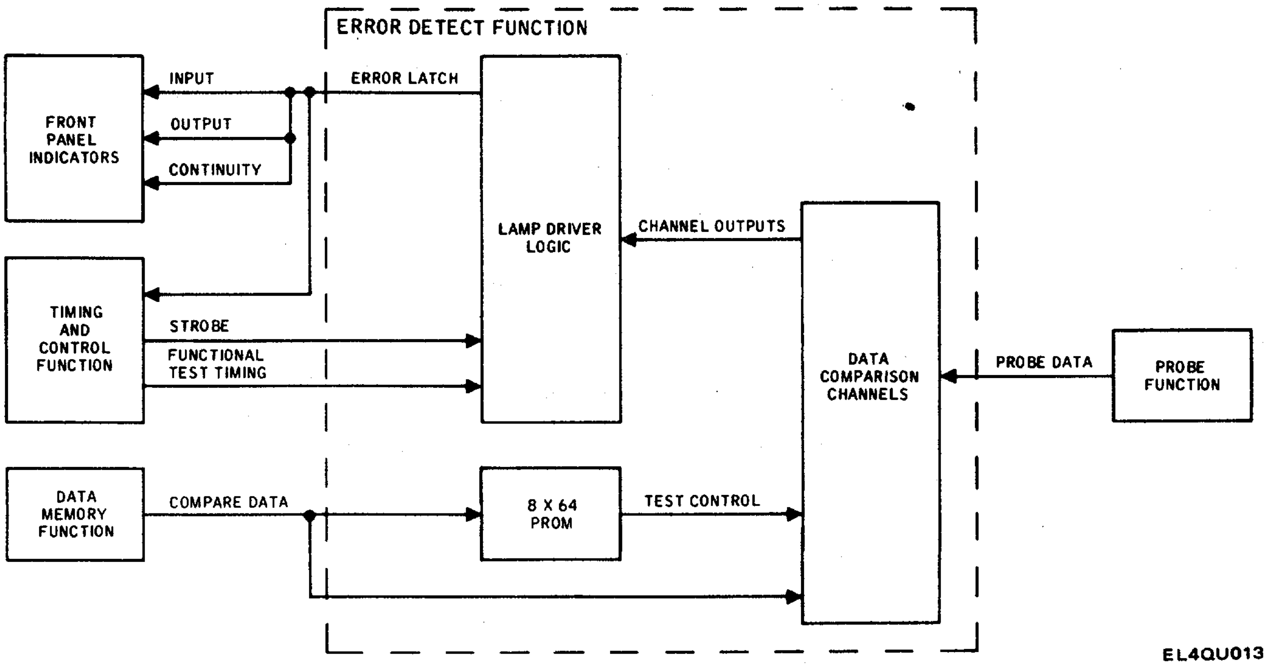


Figure 2-6. Error Detect Function Block Diagram

If no error is present during either strobe, no front panel error indicator lights.

2-12. Self-Test Function. The self-test sequence is initiated by connecting the test set probe assembly to terminal board TB1l1 (self-test strip) on the MTS front panel. The timing and control function transfers the random ID signal to the self-test detector logic (see figure 2-7). The self-test detector logic interprets the random ID signal as the self-test function. The probe-connected signal enables the card ID generator logic. The card ID generator logic is a six-bit binary counter. The output of the card ID generator logic is a dummy card ID corresponding to one of the MTS-testable cards. The output is applied to the control memory function as if the output were a true card ID. The MTS then cycles through state timing to state 7 as if an actual card were being tested. At state 7, the dummy card ID is presented to the control memory function. This action initiates the first bit of the corresponding test pattern. The probe data (72 lines) from the probe function is loaded by the functional test timing signal into the 72-bit data buffer logic. The clock signal from the 72-clock generator logic serially clocks the probe data (test pattern) into the self-test compare logic. The probe data is clocked with the clocked probe data signal. After the 72 bits of data are dumped into the self-test compare logic, the functional test timing signal loads the next bits of the test pattern into the 72-bit data buffer logic. This sequence is repeated until a complete set of test patterns for that card ID is stored in the self-test compare logic. Then, the sum of the test pattern data is compared with the stored data. If no error occurs the card ID generator logic is advanced by the functional test timing signal to the next dummy binary coded card ID and the test sequence for that card ID is initiated. This continues until all data for all of the testable cards is processed and error-checked.

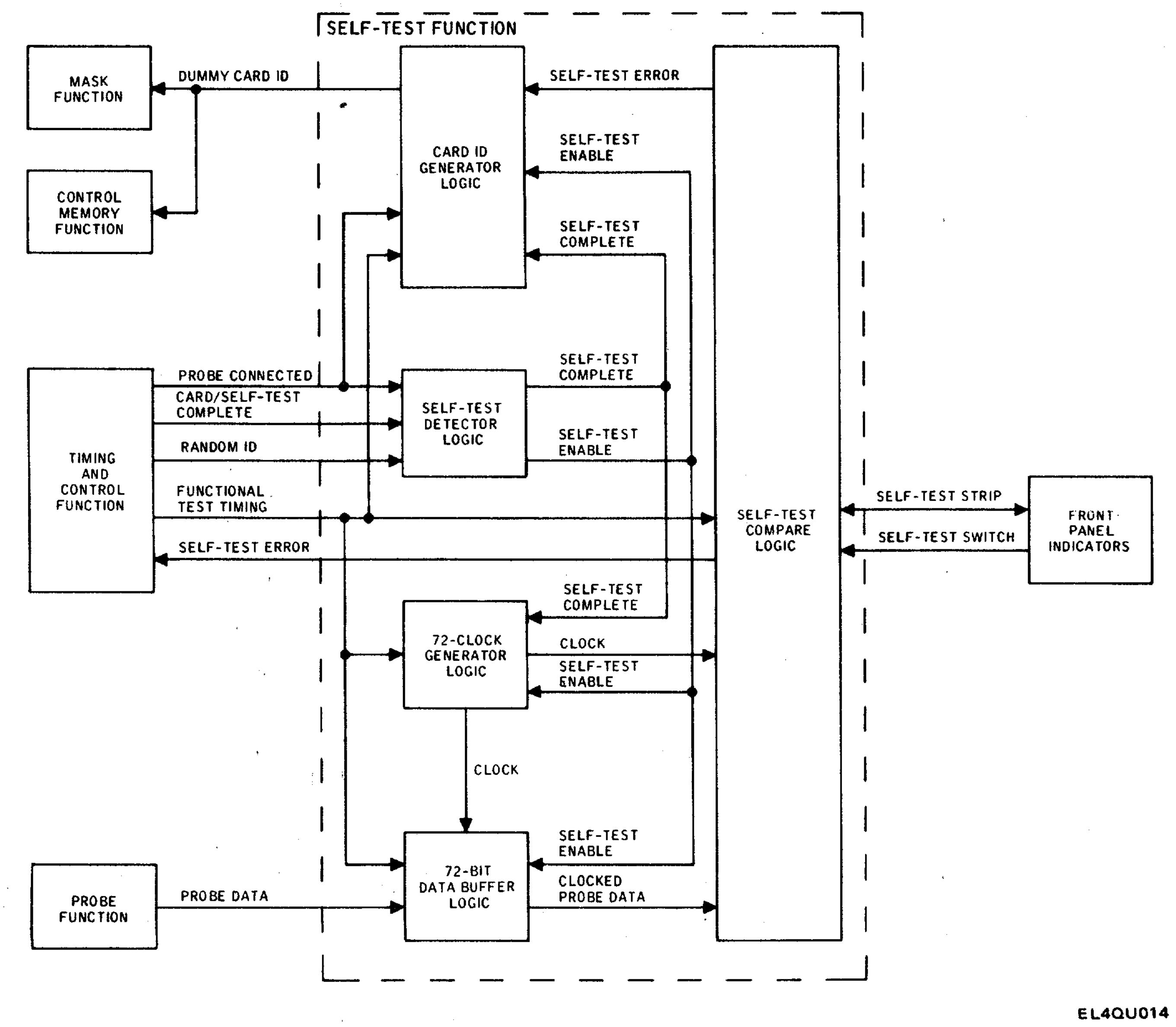


Figure 2-7. Self-Test Function Block Diagram

If an error is detected, the GO indicator goes out and the NO-GO indicator remains on. The self-test error signal causes the self-test routine to loop on the card ID where the failure occurred. To get out of this loop, the operator must press the SELF-TEST switch on the front panel. If the self-test procedure is completed with no errors detected, the NO-GO indicator goes out and the GO indicator remains, on. When the self-test is completed, the timing and control function applies the card/self-test complete signal to the self-test detect logic. The self-test detect logic then generates an internal self-test complete signal and stops the self-test function.

2-13. Probe Function. The probe function (see figure 2-8) allows interfacing with and control of the CUT. The timing and control function maintains primary control of the internal circuits of the test set probe assembly. The mask function controls the gates in the probe control logic. The probe control logic is a signal buffer and a series of gates which control the signals. The test pattern data and modem test data signals (from the data memory function) and the test clocks are applied to the input of the gates. The card reed switch control signal (from the timing and control function) and the circuit mask and I/O mask signals (from the mask function) are applied to the gate enables. The MTS logic controls timing of the gate out-puts. All data lines are terminated in special line terminator networks to keep the CUT operating normally.

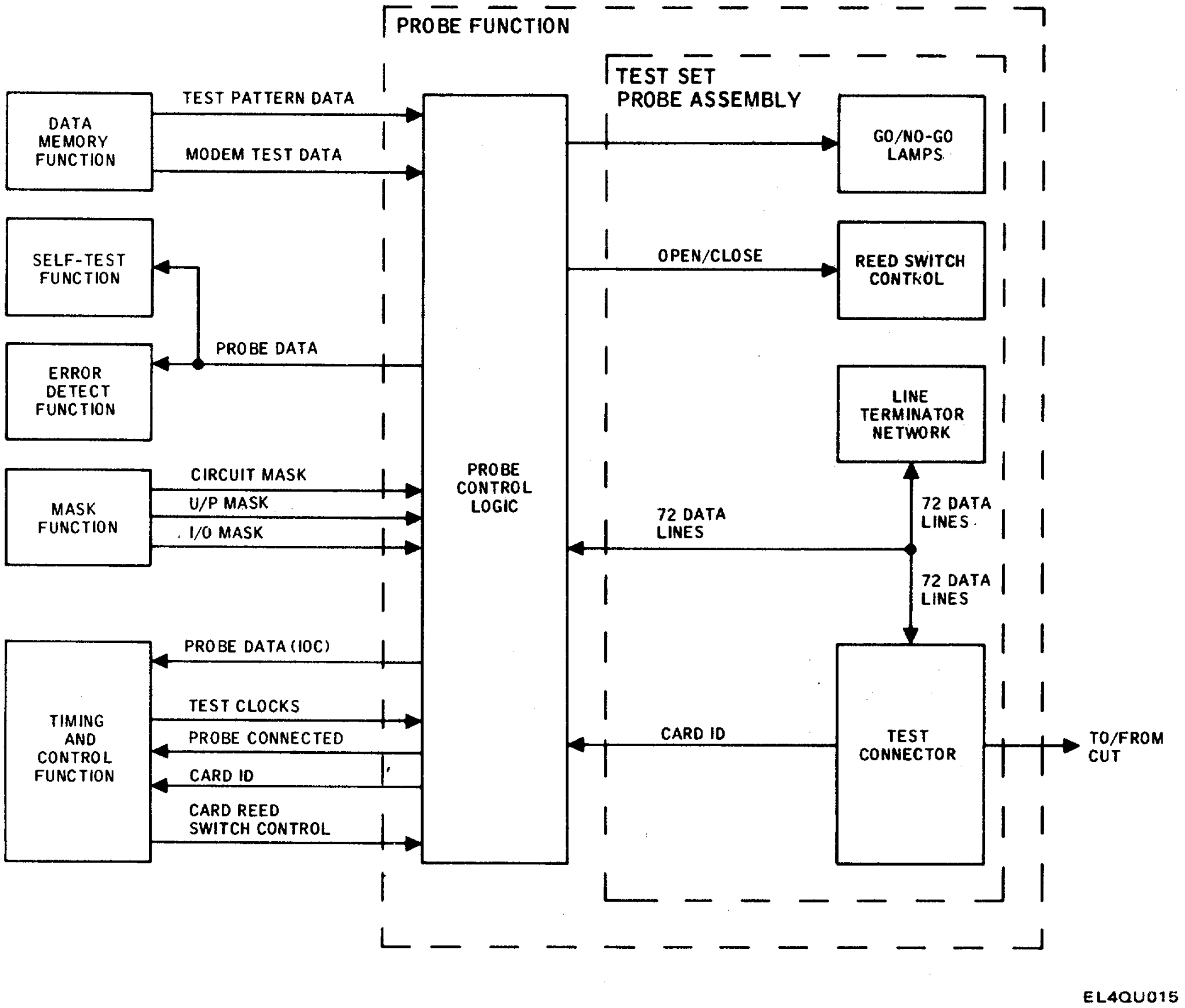


Figure 2-8. Probe function Block Diagram

a. Continuity Test. During a continuity test, the timing and control function applies a dc voltage to the CUT data lines. Continuity test results are returned (through 72 data lines) to the probe control logic, which applies the probe data signal to the error detect function or self-test function (during a self-test).

b. Functional Test. During a functional test, the reed switch control opens or closes the CUT reed switch under control of the timing and control function. Test pattern data is applied to the CUT. The functional test results are returned (through the 72 data lines) to the probe control logic. The probe control logic transfers the data to the error detect logic for comparison with stored information. Either the GO or the NO-GO indicator is turned off by the timing and control function according to the test results.

2-14. Power Function. Power to operate the MTS is provided by an external 135v power supply. The ±135v input is converted to ±5v, ±15v, +12v, +5v reserve, and +5v logic voltages by dc/dc converters PS1 and PS2. Power is distributed within the MTS as shown in figure 2-9.

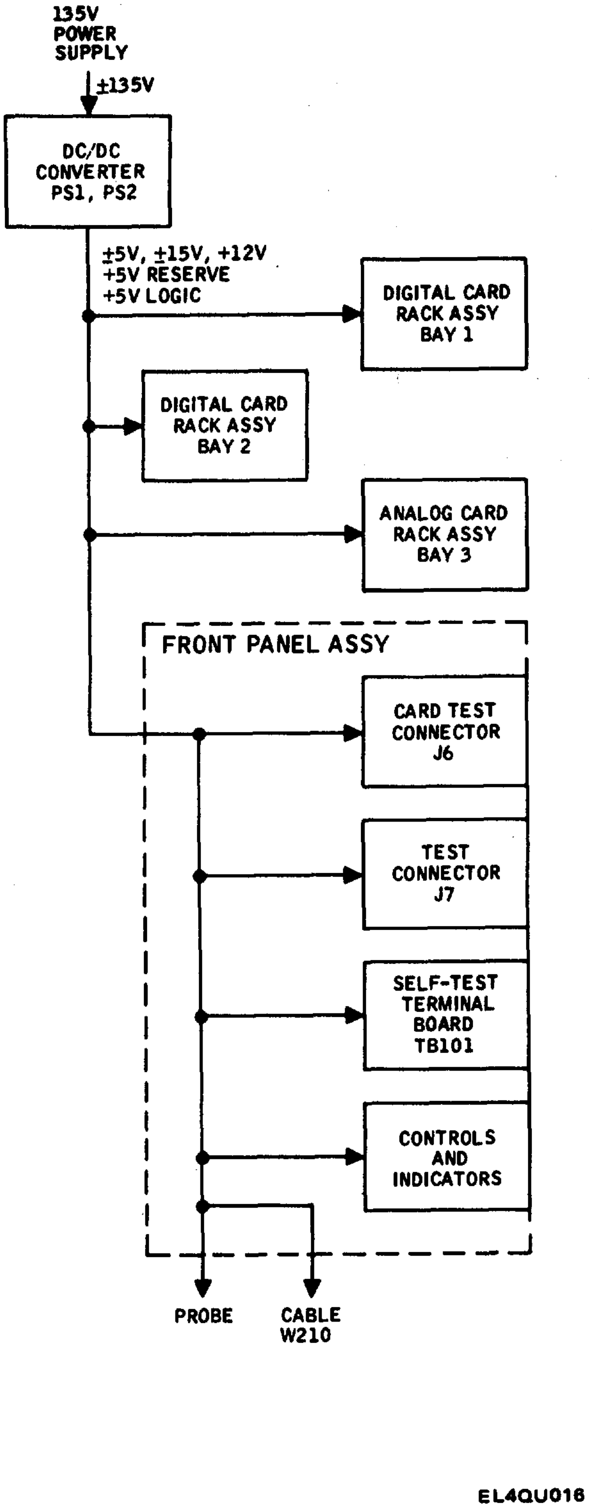


Figure 2-9. Internal Power Distribution Block Diagram

CHAPTER 3

GENERAL SUPPORT MAINTENANCE INSTRUCTIONS

Section I. INTRODUCTION

3-1. Scope. This chapter provides information and instructions for general support maintenance of the Module Test Set (MTS). The instructions contained in this chapter correspond to the maintenance functions designated in the Maintenance Allocation Chart in TM 11-7010-201-12.

3-2. Authorized Maintenance. General Support maintenance is limited by the repair parts, tools, and test equipment authorized. If a failed assembly cannot be repaired by General Support maintenance, it should be sent to the depot maintenance facility for repair.

3-3 Authorized Adjustments. General Support maintenance personnel are authorized to perform only the specific procedures of this chapter. The dc/dc converters (PS1 and PS2) contain sealed adjustable components. Adjustment of these components is authorized only at the depot level of maintenance. Do not attempt to repair equipment by performing authorized adjustments. Replace the faulty item and send the item to depot for repair.

Section II. TOOLS AND TEST EQUIPMENT

3-4. Introduction. This section lists the tools and test equipment required for General Support maintenance of the MTS.

3-5. Tools and Test Equipment Required. Information can be found in the Maintenance Allocation Chart for the MTS in TM 11-7010-201-12.

Section III. TROUBLESHOOTING

3-6. Introduction. This section consists of general troubleshooting information for General Support maintenance personnel. Troubleshooting the MTS consists primarily of performing the MTS self-test procedure (refer to TM 11-7010-201-12) and performing continuity checks on cables and wiring harnesses.

NOTE

Intermittent failures may be caused by debris in the wire-wrap assemblies or a poor cable connection. A close inspection and cleaning may correct the problem.

3-7. Wire Lists. Wire lists (see volumes 2, 3 and 4) are servicing aids for signal tracing and troubleshooting. They provide descriptive data such as connector number, type of wire, wire groups, routing, shielding, logic, mnemonics, and other information related to internal wiring. The MTS uses three types of lists - connector, string, and logic - to completely document wiring and signals. The following paragraphs describe the content and structure of these lists.

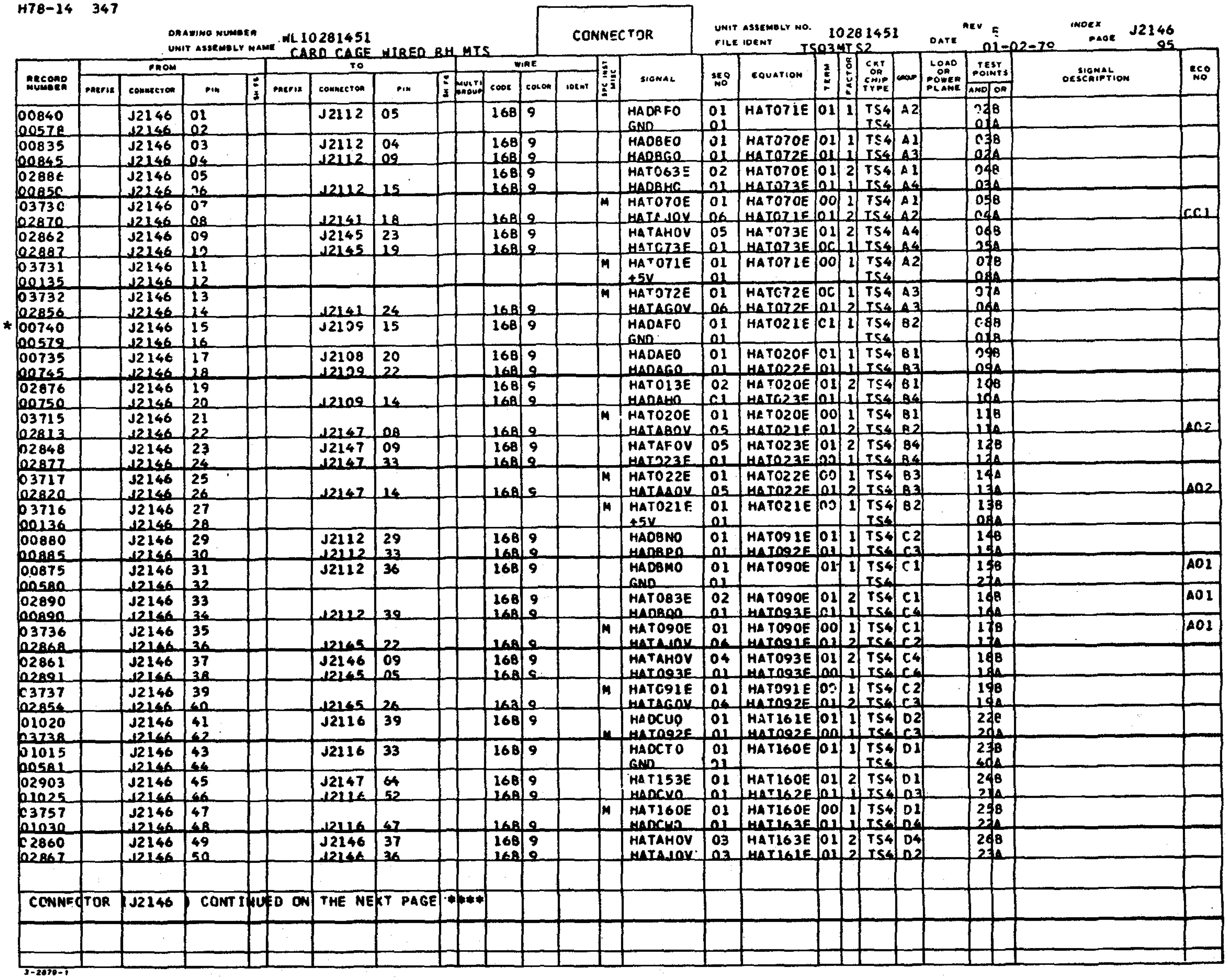
a. Connector List. The connector list furnishes a listing of all connectors in the MTS in alphanumeric order with the designated signal on each pin. Included in the list are terminal boards, ground blocks, and components mounted on the connector assembly. These parts also have the signal designations on each pin identified. Nonwired connector pins are also listed, whether unused, connected to spare circuits, or connected to spare OR gates. A typical connector list example is shown in figure 3-1. Table 3-1 explains the connector list column headings.

b. String List. The string list provides the information necessary to identify the interconnections for a specific signal designation. The list presents data according to signal designations which are given in alphanumeric sequence. The string list is useful in isolating shorts, opens, and grounds. A typical string list example is shown in figure 3-2. Table 3-2 explains the string list column headings.

c. Logic List. The logic list contains equations arranged in alphanumeric order. Logic lists are provided for each assembly containing digital circuitry. Specifically, the logic list shows the active elements, with the logic gates required to perform specific functions. Supplementary information provided by the list includes the part number of the circuit card containing the circuit elements, the specific circuit group used on the card, the location of the circuit card in the card rack, significant test points, and a brief description of the function that each equation performs. A typical logic list example is shown in figure 3-3. An explanation of the logic list is given in table 3-3.

d. Wire Information. Wire used to interconnect various cards and components within the MTS has identifying marks and codes which define the type of wire to be used during repair. Figure 3-4 shows the various types of shield terminations used in the MTS. Table 3-4 provides a list of the basic wire codes used to identify he different kinds of wire. Detailed wire information can be found in the appropriate wire list.

e. MTS Wire List Index. An index to the various connector, string and logic lists for the MTS is provided in table 3-5.



H78-14 347

DRAWING NUMBER WL10281451
UNIT ASSEMBLY NAME CARD CAGE WIRED RH MTS

CONNECTOR

UNIT ASSEMBLY NO. 10281451
FILE IDENT TSQ3MTS2
REV E
DATE 01-02-79
INDEX J2146
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RECORD NUMBER	FROM				TO					WIRE			SPC INST MISC	SIGNAL	SEQ NO	EQUATION	TERM	FACTOR	CKT OR CHIP TYPE	GROUP	LOAD OR POWER PLANE	TEST POINTS		SIGNAL DESCRIPTION	ECO NO
	PREFIX	CONNECTOR	PIN	SH FE	PREFIX	CONNECTOR	PIN	SH FE	MULTI GROUP	CODE	COLOR	IDENT										AND	OR		
00840		J2146	01			J2112	05			168	9			HADRFO	01	HAT071E	01	1	TS4	A2		02B			
00578		J2146	02											GND	01				TS4			01A			
00835		J2146	03			J2112	04			168	9			HADBEO	01	HAT070E	01	1	TS4	A1		03B			
00845		J2146	04			J2112	09			168	9			HADBGO	01	HAT072E	01	1	TS4	A3		02A			
02886		J2146	05							168	9			HAT063E	02	HAT070E	01	2	TS4	A1		04B			
00850		J2146	06			J2112	15			168	9			HADBHO	01	HAT073E	01	1	TS4	A4		03A			
03730		J2146	07										M	HAT070E	01	HAT070E	00	1	TS4	A1		05B			
02870		J2146	08			J2141	18			168	9			HATAJOV	06	HAT071E	01	2	TS4	A2		04A			CC1
02862		J2146	09			J2145	23			168	9			HATAHOV	05	HAT073E	01	2	TS4	A4		06B			
02887		J2146	10			J2145	19			168	9			HAT073E	01	HAT073E	00	1	TS4	A4		05A			
03731		J2146	11										M	HAT071E	01	HAT071E	00	1	TS4	A2		07B			
00135		J2146	12											+5V	01				TS4			08A			
03732		J2146	13										M	HAT072E	01	HAT072E	00	1	TS4	A3		07A			
02856		J2146	14			J2141	24			168	9			HATAGOV	06	HAT072E	01	2	TS4	A3		06A			
* 00740		J2146	15			J2109	15			168	9			HADAFO	01	HAT021E	C1	1	TS4	B2		08B			
00579		J2146	16											GND	01				TS4			01B			
00735		J2146	17			J2108	20			168	9			HADAEO	01	HAT020F	01	1	TS4	B1		09B			
00745		J2146	18			J2109	22			168	9			HADAGO	01	HAT022E	01	1	TS4	B3		09A			
02876		J2146	19							168	9			HAT013E	02	HAT020E	01	2	TS4	B1		10B			
00750		J2146	20			J2109	14			168	9			HADAHO	C1	HAT023E	01	1	TS4	B4		10A			
03715		J2146	21										M	HAT020E	01	HAT020E	00	1	TS4	B1		11B			
02813		J2146	22			J2147	08			168	9			HATABOV	05	HAT021E	01	2	TS4	B2		11A			A02
02848		J2146	23			J2147	09			168	9			HATAFOV	05	HAT023E	01	2	TS4	B4		12B			
02877		J2146	24			J2147	33			168	9			HAT023E	01	HAT023E	00	1	TS4	B4		12A			
03717		J2146	25										M	HAT022E	01	HAT022E	00	1	TS4	B3		14A			
02820		J2146	26			J2147	14			168	9			HATAAOV	05	HAT022E	01	2	TS4	B3		13A			A02
03716		J2146	27										M	HAT021E	01	HAT021E	00	1	TS4	B2		13B			
00136		J2146	28											+5V	01				TS4			08A			
00880		J2146	29			J2112	29			168	9			HADBNO	01	HAT091E	01	1	TS4	C2		14B			
00885		J2146	30			J2112	33			168	9			HADBPO	01	HAT092E	01	1	TS4	C3		15A			
00875		J2146	31			J2112	36			168	9			HADBMO	01	HAT090E	01	1	TS4	C1		15B			A01
00580		J2146	32											GND	01				TS4			27A			
02890		J2146	33							168	9			HAT083E	02	HAT090E	01	2	TS4	C1		16B			A01
00890		J2146	34			J2112	39			168	9			HADBQO	01	HAT093E	C1	1	TS4	C4		16A			
03736		J2146	35										M	HAT090E	01	HAT090E	00	1	TS4	C1		17B			A01
02868		J2146	36			J2145	22			168	9			HATAJOV	06	HAT091E	01	2	TS4	C2		17A			
02861		J2146	37			J2146	09			168	9			HATAHOV	04	HAT093E	01	2	TS4	C4		18B			
02891		J2146	38			J2145	05			168	9			HAT093E	01	HAT093E	00	1	TS4	C4		18A			
03737		J2146	39										M	HAT091E	01	HAT091E	00	1	TS4	C2		19B			
02854		J2146	40			J2145	26			168	9			HATAGOV	06	HAT092E	01	2	TS4	C3		19A			
01020		J2146	41			J2116	39			168	9			HADCUO	01	HAT161E	01	1	TS4	D2		22B			
03738		J2146	42										M	HAT092E	01	HAT092E	00	1	TS4	C3		20A			
01015		J2146	43			J2116	33			168	9			HADCTO	01	HAT160E	01	1	TS4	D1		23B			
00581		J2146	44											GND	01				TS4			40A			
02903		J2146	45			J2147	64			168	9			HAT153E	01	HAT160E	01	2	TS4	D1		24B			
01025		J2146	46			J2116	52			168	9			HADCVO	01	HAT162E	01	1	TS4	D3		21A			
03757		J2146	47										M	HAT160E	01	HAT160E	00	1	TS4	D1		25B			
01030		J2146	48			J2116	47			168	9			HADCWO	01	HAT163E	01	1	TS4	D4		22A			
02860		J2146	49			J2146	37			168	9			HATAHOV	03	HAT163E	01	2	TS4	D4		26B			
02867		J2146	50			J2146	36			168	9			HATAJOV	03	HAT161E	01	2	TS4	D2		23A			

CONNECTOR (J2146) CONTINUED ON THE NEXT PAGE ****

3-2870-1

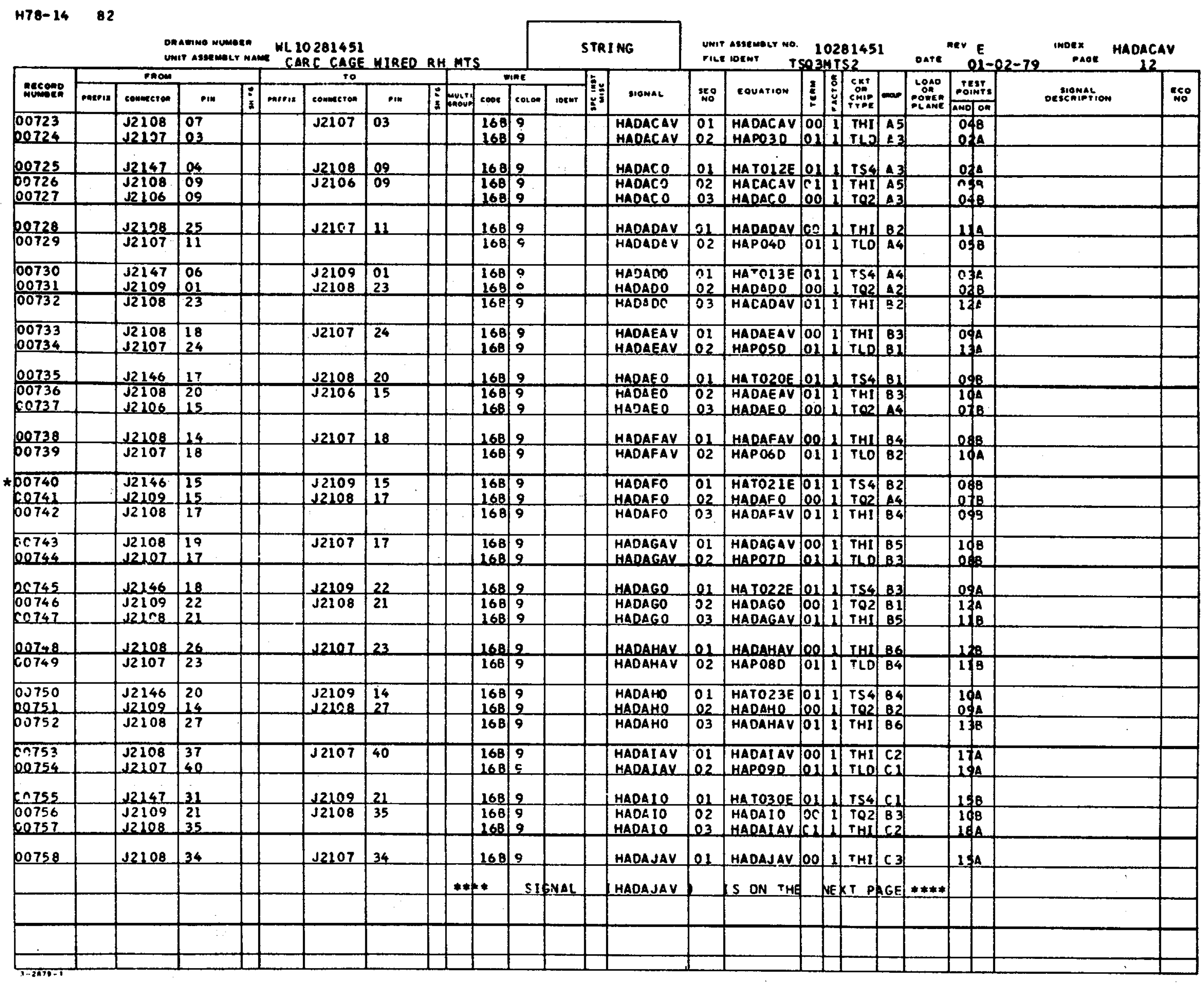
Figure 3-1. Connector List Example

Table 3-1. Connector List Column Explanations

Column heading	Explanation
RECORD NUMBER	Not used by maintenance personnel
FROM	Originating end of wire
PREFIX	When used, alphanumeric indicating when wire terminates in two assemblies
CONNECTOR	Any type of terminating point, plug, receptacle
PIN	Exact originating point of respective connector
SH. FIG.	When used, references illustration (figure 3-4) showing how shielded wire or coax is to be terminated. Number in these fields indicates level of automatic wire wrapping
TO	Terminating end of wire
PREFIX	Same as FROM prefix
CONNECTOR	Same as FROM connector
PIN	Same as FROM pin
SH.FIG.	Same as FROM sh. fig.
WIRE	
MULTIGROUP	Associates wire of group such as twisted wire or shielded wire. Jacket, pigtails, and center conductor are shown as common group
CODE	Three-digit code for wire type and gage or bus bar
COLOR	Color according to standard RETMA color code: base color, stripe 1, and stripe 2. If single number used, wire is solid color; if two numbers, wire has one stripe; if three numbers, two stripes
IDENT	Number stamped on wire or sleeving to differentiate it from another. Not used in all wiring
SPC. INST. MISC	Code which indicates that wire must be given special attention as follows: A-Direct routing with no service loops or harnessing F-Refer to Signal Description column for this line

Table 3-1. Connector List Column Explanations - Continued

Column heading	Explanation
	G-This connection does not go direct to TO connector but intersects wire going to TO connector I -Junction point for multiple laminate board, i.e., printed circuit card connections J -Designates bus reference point
SIGNAL	Alphanumeric signal name (mnemonic where feasible) which differentiates one specific function from another
SEQ. NO.	Not used by maintenance personnel
EQUATION	Symbolic name (significant where feasible) which identifies logic equation driven by signal
TERM	Designates whether signal is output (00) or input (01)
FACTOR	Designates order in which signal is listed in FACTOR column of logic list
CKT OR CHIP TYPE	Indicates type of card in slot
GROUP	Designates specific element of IC chip
LOAD OR POWER PLANE	Not used by maintenance personnel
TEST POINTS	Letter or numerical which indicates AND (input signal) test point if located on left side of column or OR (output signal) test point if located on right side
SIGNAL DESCRIPTION	Abbreviated description or name of signal or voltage
ECO NO.	Letter-number combination to show ECO level of specific wire list



H78-14 82

DRAWING NUMBER WL10281451

UNIT ASSEMBLY NAME CARC CAGE WIRED RH MTS

STRING

UNIT ASSEMBLY NO. 10281451

FILE IDENT TSQ3MTS2

REV E

DATE 01-02-79

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RECORD NUMBER	FROM				TO				WIRE				SPC INST MISC	SIGNAL	SEQ NO	EQUATION	TERM	FACTOR	CKT OR CHIP TYPE	GROUP	LOAD OR POWER PLANE	TEST POINTS		SIGNAL DESCRIPTION	ECO NO
	PREFIX	CONNECTOR	PIN	SH FG	PREFIX	CONNECTOR	PIN	SH FG	MULTI GROUP	CODE	COLOR	IDENT										AND	OR		
00723		J2108	07			J2107	03			16B	9			HADACAV	01	HADACAV	00	1	THI	A5		04B			
00724		J2107	03							16B	9			HADACAV	02	HAP03D	01	1	TLD	A3		02A			
00725		J2147	04			J2108	09			16B	9			HADACO	01	HAT012E	01	1	TS4	A3		02A			
00726		J2108	09			J2106	09			16B	9			HADACO	02	HACACAV	01	1	THI	A5		05B			
00727		J2106	09							16B	9			HADACO	03	HADACO	00	1	TQ2	A3		04B			
00728		J2108	25			J2107	11			16B	9			HADADAV	01	HADADAV	00	1	THI	B2		11A			
00729		J2107	11							16B	9			HADADAV	02	HAP04D	01	1	TLD	A4		05B			
00730		J2147	06			J2109	01			16B	9			HADADO	01	HAT013E	01	1	TS4	A4		03A			
00731		J2109	01			J2108	23			16B	9			HADADO	02	HADADO	00	1	TQ2	A2		02B			
00732		J2108	23							16B	9			HADADO	03	HACADAV	01	1	THI	B2		12A			
00733		J2108	18			J2107	24			16B	9			HADAEAV	01	HADAEAV	00	1	THI	B3		09A			
00734		J2107	24							16B	9			HADAEAV	02	HAP05D	01	1	TLD	B1		13A			
00735		J2146	17			J2108	20			16B	9			HADAEO	01	HAT020E	01	1	TS4	B1		09B			
00736		J2108	20			J2106	15			16B	9			HADAEO	02	HADAEAV	01	1	THI	B3		10A			
00737		J2106	15							16B	9			HADAEO	03	HADAEO	00	1	TQ2	A4		07B			
00738		J2108	14			J2107	18			16B	9			HADAFAV	01	HADAFAV	00	1	THI	B4		08B			
00739		J2107	18							16B	9			HADAFAV	02	HAP06D	01	1	TLD	B2		10A			
*00740		J2146	15			J2109	15			16B	9			HADAFO	01	HAT021E	01	1	TS4	B2		08B			
00741		J2109	15			J2108	17			16B	9			HADAFO	02	HADAFO	00	1	TQ2	A4		07B			
00742		J2108	17							16B	9			HADAFO	03	HADAFAV	01	1	THI	B4		09B			
00743		J2108	19			J2107	17			16B	9			HADAGAV	01	HADAGAV	00	1	THI	B5		10B			
00744		J2107	17							16B	9			HADAGAV	02	HAP07D	01	1	TLD	B3		08B			
00745		J2146	18			J2109	22			16B	9			HADAGO	01	HAT022E	01	1	TS4	B3		09A			
00746		J2109	22			J2108	21			16B	9			HADAGO	02	HADAGO	00	1	TQ2	B1		12A			
00747		J2108	21							16B	9			HADAGO	03	HADAGAV	01	1	THI	B5		11B			
00748		J2108	26			J2107	23			16B	9			HADAHAV	01	HADAHAV	00	1	THI	B6		12B			
00749		J2107	23							16B	9			HADAHAV	02	HAP08D	01	1	TLD	B4		11B			
00750		J2146	20			J2109	14			16B	9			HADAHO	01	HAT023E	01	1	TS4	B4		10A			
00751		J2109	14			J2108	27			16B	9			HADAHO	02	HADAHO	00	1	TQ2	B2		09A			
00752		J2108	27							16B	9			HADAHO	03	HADAHAV	01	1	THI	B6		13B			
00753		J2108	37			J2107	40			16B	9			HADAIAV	01	HADAIAV	00	1	THI	C2		17A			
00754		J2107	40							16B	9			HADAIAV	02	HAP09D	01	1	TLD	C1		19A			
00755		J2147	31			J2109	21			16B	9			HADAIO	01	HAT030E	01	1	TS4	C1		15B			
00756		J2109	21			J2108	35			16B	9			HADAIO	02	HADAIO	00	1	TQ2	B3		10B			
00757		J2108	35							16B	9			HADAIO	03	HADAIAV	01	1	THI	C2		18A			
00758		J2108	34			J2107	34			16B	9			HADAJAV	01	HADAJAV	00	1	THI	C3		15A			
										****	SIGNAL			(HADAJAV)		IS ON THE			NEXT PAGE		****				

3-2879-1

Figure 3-2. String List Example

Table 3-2. String List Column Explanations

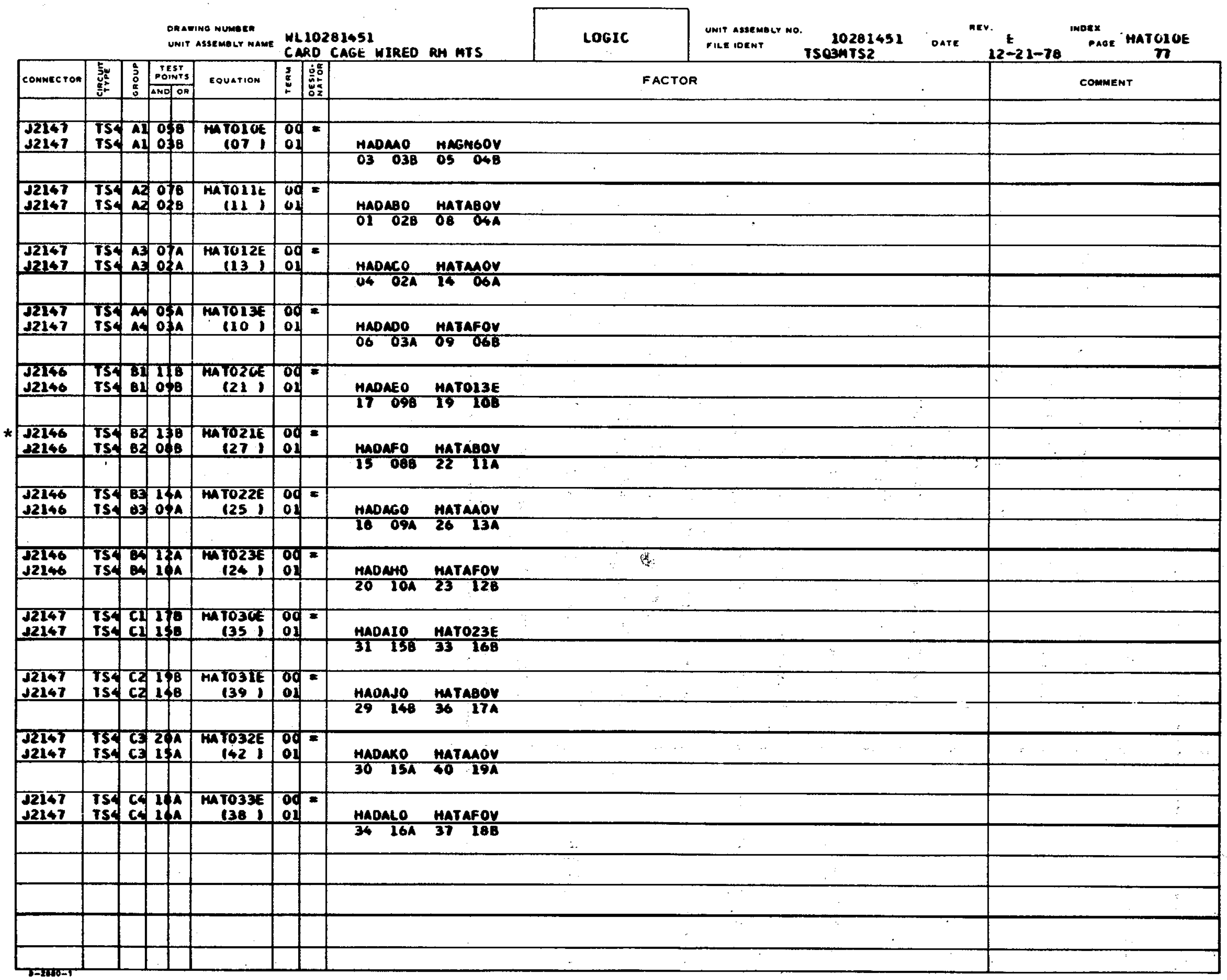
Column heading	Explanation
RECORD NUMBER	Not used by maintenance personnel
FROM	Originating end of wire
PREFIX	When used, alphanumeric indicating when wire terminates in two assemblies
CONNECTOR	Any type of terminating point, plug, or receptacle
PIN	Exact originating point of respective connector. Designations are: A-SHXXX indicates junction of shield and pigtail, four right-most digits being wire identity of shielded wire B-JCT indicates common point of two or more shield pigtails C-Jacket is term used when describing line that defines identification of shielded wire
SH. FIG.	When used, references graphic representation (figure 3-4) showing how shielded wire or coax is to be terminated. Number in these fields indicates level of automatic wire wrapping
TO	Terminating end of wire
PREFIX	Same as FROM prefix
CONNECTOR	Same as FROM connector
PIN	Same as FROM pin
SH. FIG.	Same as FROM sh. fig.
WIRE	
MULTIGROUP	Associates wire of group such as twisted wire or shielded wire. Jacket, pigtails, and center conductor are shown as common group
CODE	Three-digit code for wire type and gage or bus bar
COLOR	Color according to standard RETMA color code: base color, stripe 1, and stripe 2. If single number used, wire is solid color; if two numbers9, wire has one stripe; if three numbers, two stripes

Table 3-2. String List Column Explanations

Column heading	Explanation
IDENT.	Number stamped on wire or sleeving to differentiate it from another. Not used in all wiring
SLEEVE	Not used
SPC. INST.	Code which indicates that wire must be given special attention as follows: A-Direct routing with no service loops or harnessing F-Refer to Signal Description column for this line G-Connection does not go direct to TO connector but intersects wire going to TO connector I-Junction point for multiple laminate board, i.e., printed circuit card connections J-Designates bus reference point
SIGNAL	Alphanumeric signal name (mnemonic where feasible) which differentiates one specific function from another SPP Denotes available termination SPW Denotes nonfunctional wire that is terminated at one or both ends SPF Denotes unwired termination that has-assigned use. Not used for maintenance SPO Denotes spare output of circuit DNW Indicates that termination may not be wired SPA Denotes unassigned circuit, one of group on circuit card SPI Indicates spare input of circuit card SPG Indicates unassigned logic gate on circuit card SPR Indicates spare resistor SPD Indicates unassigned diode of assigned gate

Table 3-2. String List Column Explanations

Column heading	Explanation
STRING SEQ. NO.	Not used for maintenance
EQUATION	Symbolic name (significant where feasible) which identifies logic equation driven by signal
TERM	Designates whether signal is output (00) or input (01)
FACTOR	Designates order in which signal is listed in FACTOR column of logic list
CKT OR CHIP TYPE	Indicates type of card in slot
GROUP	Designates specific element of IC chip
LOAD OR POWER PLANE	Not used by maintenance personnel
TEST POINTS	Letter or numerical which indicates AND (input signal) test point if located on left side of column or OR (output signal) test point if located on right side
SIGNAL DESCRIPTION	Written description or name of signal or voltage
ECO NO.	Letter-number combination to shown ECO level of specific wire list



DRAWING NUMBER WL10281451
UNIT ASSEMBLY NAME CARD CAGE WIRED RH MTS

LOGIC

UNIT ASSEMBLY NO. 10281451
FILE IDENT TSQ3MTS2
REV. E
DATE 12-21-78
INDEX HAT010E
PAGE 77

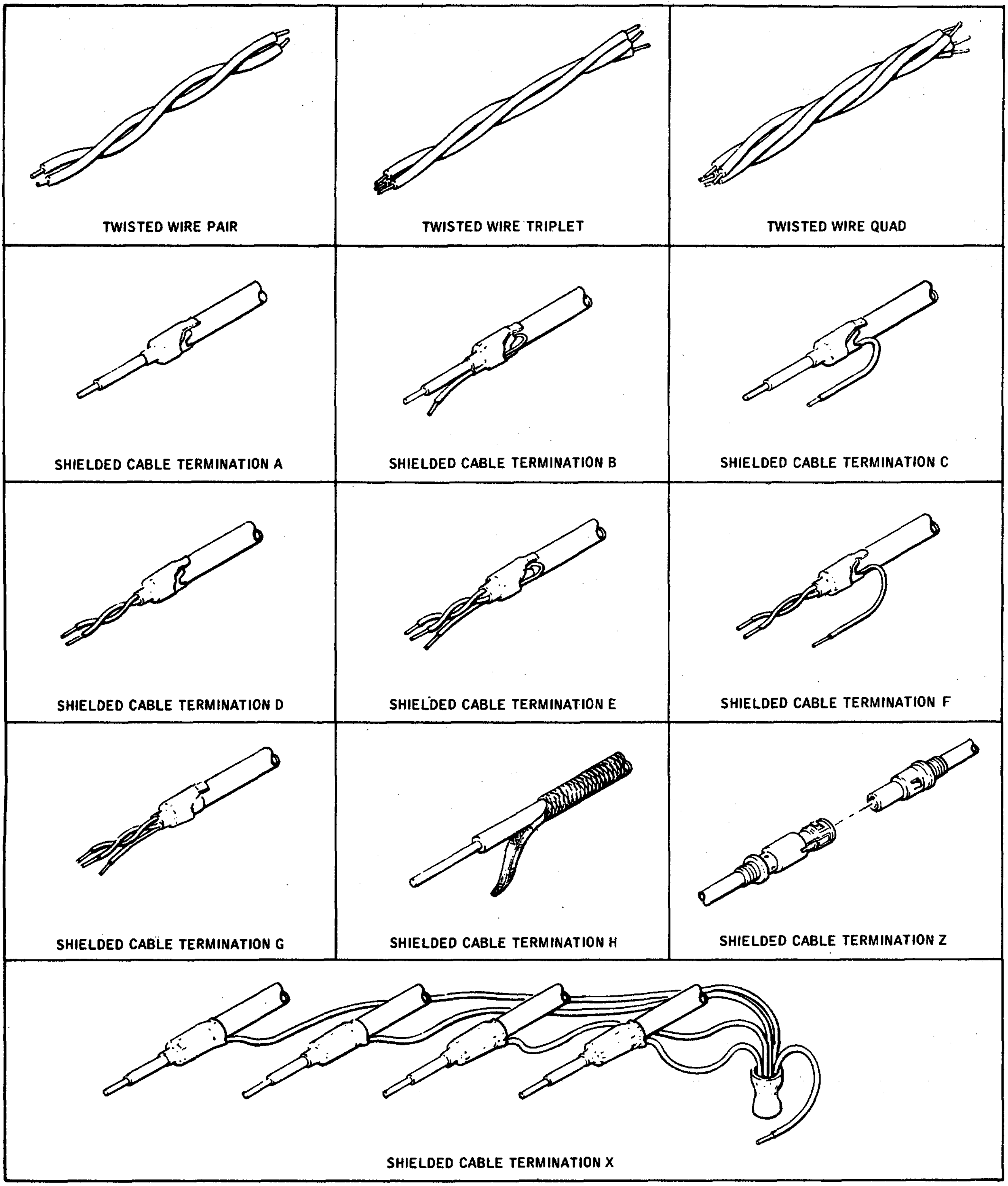
CONNECTOR	CIRCUIT TYPE	GROUP	TEST POINTS AND OR	EQUATION	TERM	DESIGNATOR	FACTOR	COMMENT
J2147	TS4	A1	05B	HAT010E	00	=		
J2147	TS4	A1	03B	(07)	01		HADAA0 HAGN60V	
							03 03B 05 04B	
J2147	TS4	A2	07B	HAT011E	00	=		
J2147	TS4	A2	02B	(11)	01		HADAB0 HATAB0V	
							01 02B 08 04A	
J2147	TS4	A3	07A	HAT012E	00	=		
J2147	TS4	A3	02A	(13)	01		HADAC0 HATAA0V	
							04 02A 14 06A	
J2147	TS4	A4	05A	HAT013E	00	=		
J2147	TS4	A4	03A	(10)	01		HADAD0 HATAF0V	
							06 03A 09 06B	
J2146	TS4	B1	11B	HAT020E	00	=		
J2146	TS4	B1	09B	(21)	01		HADAE0 HAT013E	
							17 09B 19 10B	
* J2146	TS4	B2	13B	HAT021E	00	=		
J2146	TS4	B2	08B	(27)	01		HADAF0 HATAB0V	
							15 08B 22 11A	
J2146	TS4	B3	14A	HAT022E	00	=		
J2146	TS4	B3	09A	(25)	01		HADAG0 HATAA0V	
							18 09A 26 13A	
J2146	TS4	B4	12A	HAT023E	00	=		
J2146	TS4	B4	10A	(24)	01		HADAH0 HATAF0V	
							20 10A 23 12B	
J2147	TS4	C1	17B	HAT030E	00	=		
J2147	TS4	C1	15B	(35)	01		HADAI0 HAT023E	
							31 15B 33 16B	
J2147	TS4	C2	19B	HAT031E	00	=		
J2147	TS4	C2	14B	(39)	01		HADAJ0 HATAB0V	
							29 14B 36 17A	
J2147	TS4	C3	20A	HAT032E	00	=		
J2147	TS4	C3	15A	(42)	01		HADAK0 HATAA0V	
							30 15A 40 19A	
J2147	TS4	C4	18A	HAT033E	00	=		
J2147	TS4	C4	16A	(38)	01		HADAL0 HATAF0V	
							34 16A 37 18B	

B-2880-1

Figure 3-3. Logic List Example

Table 3-3. String List Column Explanations

Column heading	Explanation
CONNECTOR	Denotes specific location for printed circuit card
CIRCUIT TYPE	Denotes specific circuit card type
GROUP	Denotes specific circuit on printed circuit card
AND	Denotes input test point or pin for specific circuit on printed circuit card
OR	Denotes output test point or pin for specific circuit on printed circuit card
EQUATION	Six alphanumeric characters which identify elements of logic units: First character: unit in which that function is located Second character: denotes functional circuit Third, fourth, and fifth characters: define specific elements involved Sixth character: designates type of input or output involved
TERM	OR function composed of one or more factors
DESIGNATOR	Arithmetic sign expressing function: = Logically equal + OR function / Directly wired to , Input received directly from gate located on same card
FACTOR	Specific input to logical gate or active element. Several factors (either ANDed or ORed together) may be used to mechanize input to equation
COMMENT	Word description of logical function performed by element or factors



TWISTED WIRE PAIR
TWISTED WIRE TRIPLET
TWISTED WIRE QUAD
SHIELDED CABLE TERMINATION A
SHIELDED CABLE TERMINATION B
SHIELDED CABLE TERMINATION C
SHIELDED CABLE TERMINATION D
SHIELDED CABLE TERMINATION E
SHIELDED CABLE TERMINATION F
SHIELDED CABLE TERMINATION G
SHIELDED CABLE TERMINATION H
SHIELDED CABLE TERMINATION Z
SHIELDED CABLE TERMINATION X

Figure 3-4. Wiring Terminations

Table 3-4. Wire Codes

Wire Code[1]	Wire type
01X	Uninsulated Bus
05X	Integral Component Lead (all gages)
14X	MIL-W-16878 Type E Wire (Teflon)
16X	898041-0002 Automatic Wrapping Wire
32X	MIL-W-16878/1 Wire (Shielded)
33X	MIL-W-16878 Type E Wire (Shielded)
42X	MIL-W-16878 Type D Twisted Wire Pair
45X	Twisted Wire Pair
46X	Twisted Wire Triplet
47X	Twisted Wire Quad
48X	Twisted Wire Pair (Cable)
50X	Twisted Wire Pair (Shielded)
52X	Twisted Wire Pair (Shielded Drum Cable)
62X	Twisted Wire Triplet (Shielded Teflon Insulation)
70X	Twisted Wire Quad (Shielded)
C0X	Coaxial Cable

[1] Third digit (X) in wire code indicates wire gage or coaxial cable type and is explained in the individual wire lists.

Table 3-5. MTS Wire List Index

Title	Drawing number	Manual number
Probe Assembly, Test Set - Wire List; String, and Connector	WL10281447	TM 11-7010-201-40-2
Test Assembly, Plug-In Unit, Wired, Wire List; String	WL10281449	TM 11-7010-201-40-2
Card Rack Assembly - Digital, RH, Wire List; String, Connector, and Logic	WL10281451	TM 11-7010-201-40-3
Card Rack Assembly - Test Set, Digital, LH, Wire List; String, Connector, and Logic	WL10281452	TM 11-7010-201-40-4
Card Rack Assembly - Analog, Wire List; String and Connector	WL10281453	TM 11-7010-201-40-2

3-8. Wiring Fault Isolation. If a malfunction occurs in the wiring harness, cabling, or circuit card connectors, remove all circuit cards and disconnect all cable connectors. Use the wire lists to check wiring in the following example:

WARNING

> HIGH VOLTAGE is used in the operation of this equipment. DEATH ON CONTACT may result if personnel fail to observe safety precautions. Learn the areas containing high voltage in each piece of equipment. Be careful not to contact high voltage connections when installing or operating this equipment.
>
> Before working inside the equipment, turn power off and ground points of high potential before touching them.

a. If signal name is unknown, use string list (see figure 3-2) to identify signal. Locate connector and pin number in the FROM column (J2146, pin 15), then find the signal name under the SIGNAL column (HADAFO) to the right of connector and pin number.

b. Check continuity between connections indicated under CONNECTOR and PIN headings in FROM column (J2146, pin 15) and connections indicated under CONNECTOR and PIN headings in TO column (J2109, pin 15). Check continuity for each listing of signal (HADAFO) in SIGNAL column.

c. To use the logic list, refer to the connector list example (see figure 3-1) or string list example (see figure 3-2), and locate in the EQUATION column HAT021E. Proceed to logic list example (see figure 3-3) and locate in the EQUATION column HAT021E. The FACTOR column identifies the logic factors needed to generate specific functions.

3-9. Cable Assemblies Fault Isolation. If equipment malfunctions cannot be corrected by performing all other normal fault isolation (FI) procedures, a defective cable assembly (W552, W553, W554, or W556) may be the cause. One method for making this determination is by cable assembly substitution. The general procedure for this consists of first disconnecting a suspected cable assembly (but leaving it in place), then obtaining a replacement cable assembly and stringing it out in the most direct route from unit to unit. If the replacement cable corrects the problem, the defective cable should be removed and the replacement installed in accordance with the appropriate procedure in section IV. A second method is to test the cable assembly following the appropriate procedure in section V. An overall cabling diagram for the MTS is shown in FO-3 (in back of manual).

Section IV. MAINTENANCE

3-10. Introduction. This section provides removal, replacement, and repair procedures for those items authorized for General Support maintenance.

WARNING

> HIGH VOLTAGE is used in the operation of this equipment. DEATH ON CONTACT may result if personnel fail to observe safety precautions. Learn the areas containing high voltage in each piece of equipment. Be careful not to contact high voltage connections when installing or operating this equipment.
>
> Before working inside the equipment, turn power off and ground points of high potential before touching them.

3-1 1. MTS Component Access. Perform the following procedure to gain access to MTS internal components (figure 3-5):

a. *Extention* Extend MTS as follows:

(1) Release eight captive screws securing front panel to case.

WARNING

> When extending the MTS, always provide support for both the MTS and the case. Extension of the MTS causes an unbalanced condition and the assembly may tip forward causing personnel injury and equipment damage.

(2) Slowly slide frame out of case until slide locks engage.

b. Retraction Retract MTS as follows:

(1) Release slide locks and carefully slide frame into case.

(2) Secure front panel to case using eight captive screws.

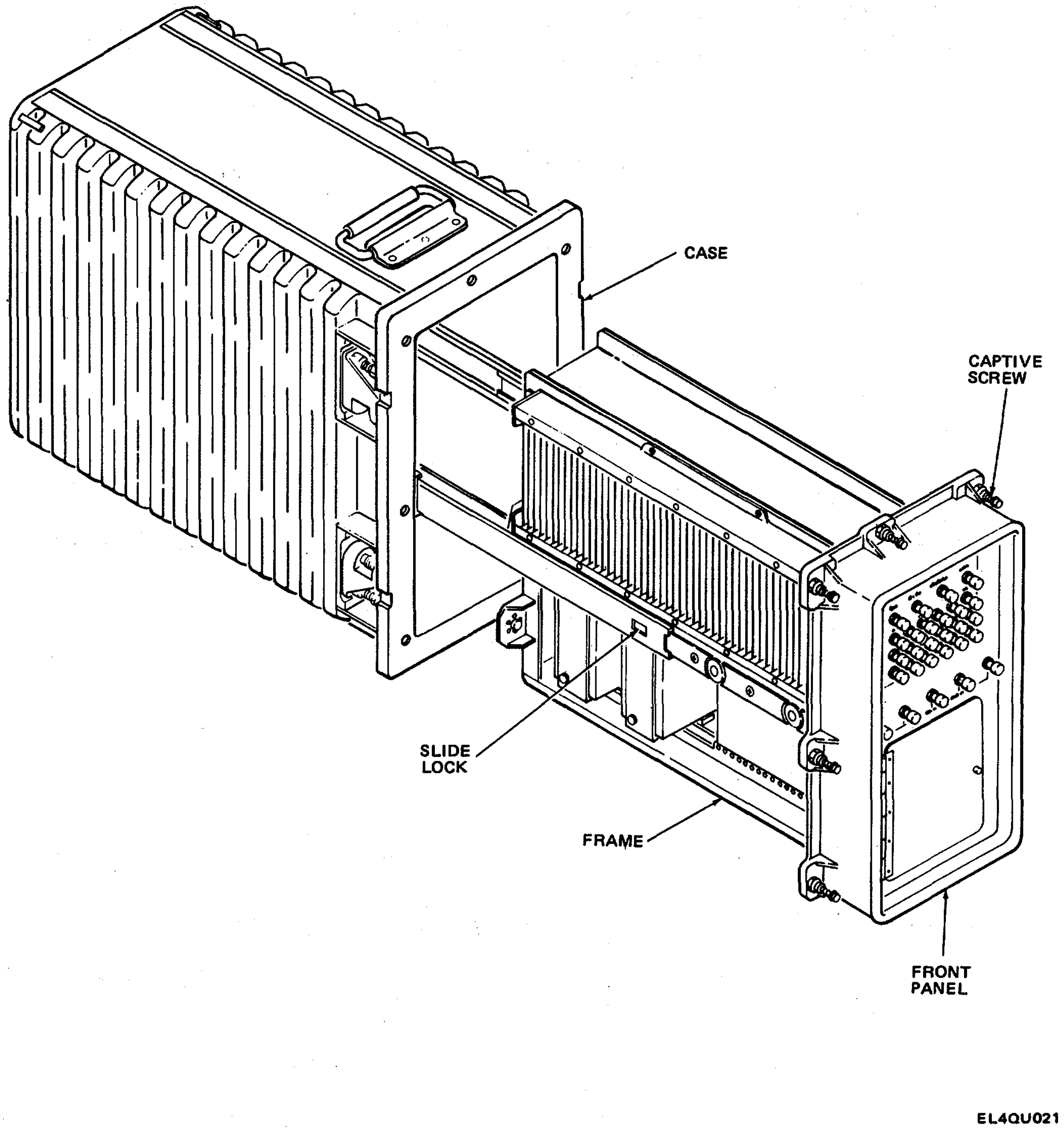


Figure 3-5. MTS Component Access

3-12. Front Panel Component Access. Perform the following procedure to gain access to rear of components mounted on the front panel (figure 3-6).

a. *Removal*. Remove front panel as follows:

(1) Extend MTS from case following procedure of paragraph 3-11.

CAUTION

Maintain support of the front panel when removed to prevent damage to the wiring harness. The wiring harness will not support the full weight of the front panel.

(2) Remove six bolts and six flat washers securing front panel to frame.

(3) Carefully remove front panel from frame.

b. Replacement. Replace front panel as follows:

(1) Place front panel in position on frame.

(2) Secure front panel to frame using six bolts and six flat washers.

3-13. Indicator and Switch-indicator Removal and Replacement. Perform the following procedure to remove and replace an indicator or switch-indicator (figure 3-7).

a. Removal Remove indicator or switch-indicator as follows:

(1) Gain access to rear of front panel following procedure of paragraph 3-12.

(2) Locate, tag, and unsolder wires connected to indicator or switch-indicator terminals.

(3) Unscrew and remove lens and lamp.

(4) Unscrew and remove sealing boot securing indicator or switch-indicator to front panel.

(5) Remove indicator or switch-indicator from front panel.

b. Replacement. Replace indicator or switch-indicator as follows:

NOTE

Use mounting hardware supplied with indicator or switch-indicator.

(1) Ensure that nut on indicator or switch-indicator is bottomed against housing.

(2) Place lockwasher over threads and install indicator or switch-indicator through hole in front panel from rear.

(3) Secure indicator or switch-indicator to front panel using sealing boot.

NOTE

Boot must seal against the surface of the front panel. Do not distort the sealing boot.

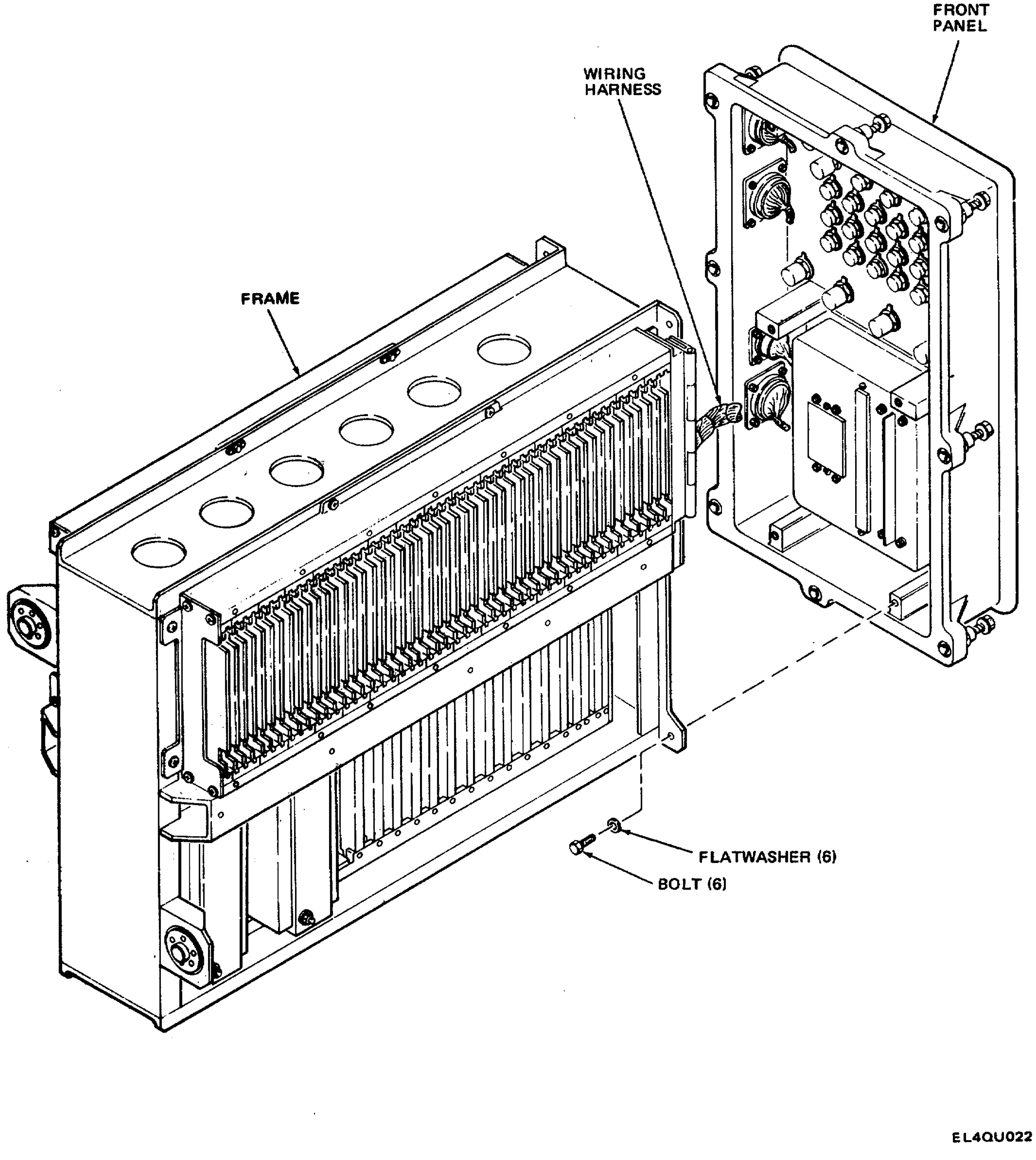


Figure 3-6. *Front Panel Component Access*

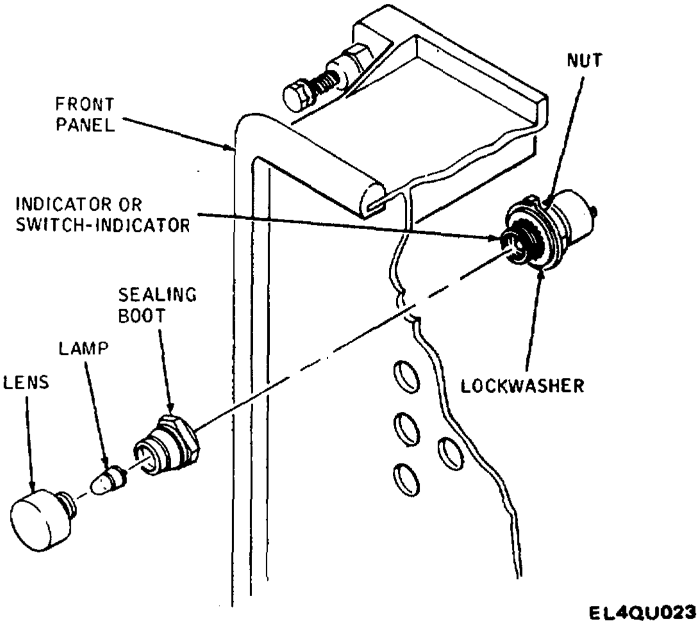


Figure 3-7. Indicator and Switch-Indicator Removal and Replacement

(4) Replace lens and lamp and secure finger-tight.

(5) Solder tagged wires to new indicator or switch-indicator and remove tags.

(6) Secure front panel to frame following procedure of paragraph 3-12.

3-14. Cable Assemblies W552, W553, and W554 Removal and Replacement. Perform the following procedure to remove and replace cable assemblies W552, W553, or W554 (figure 3-8).

a. *Removal.* Remove cable assembly as follows:

(1) Extend MTS from case following procedure of paragraph 3-11.

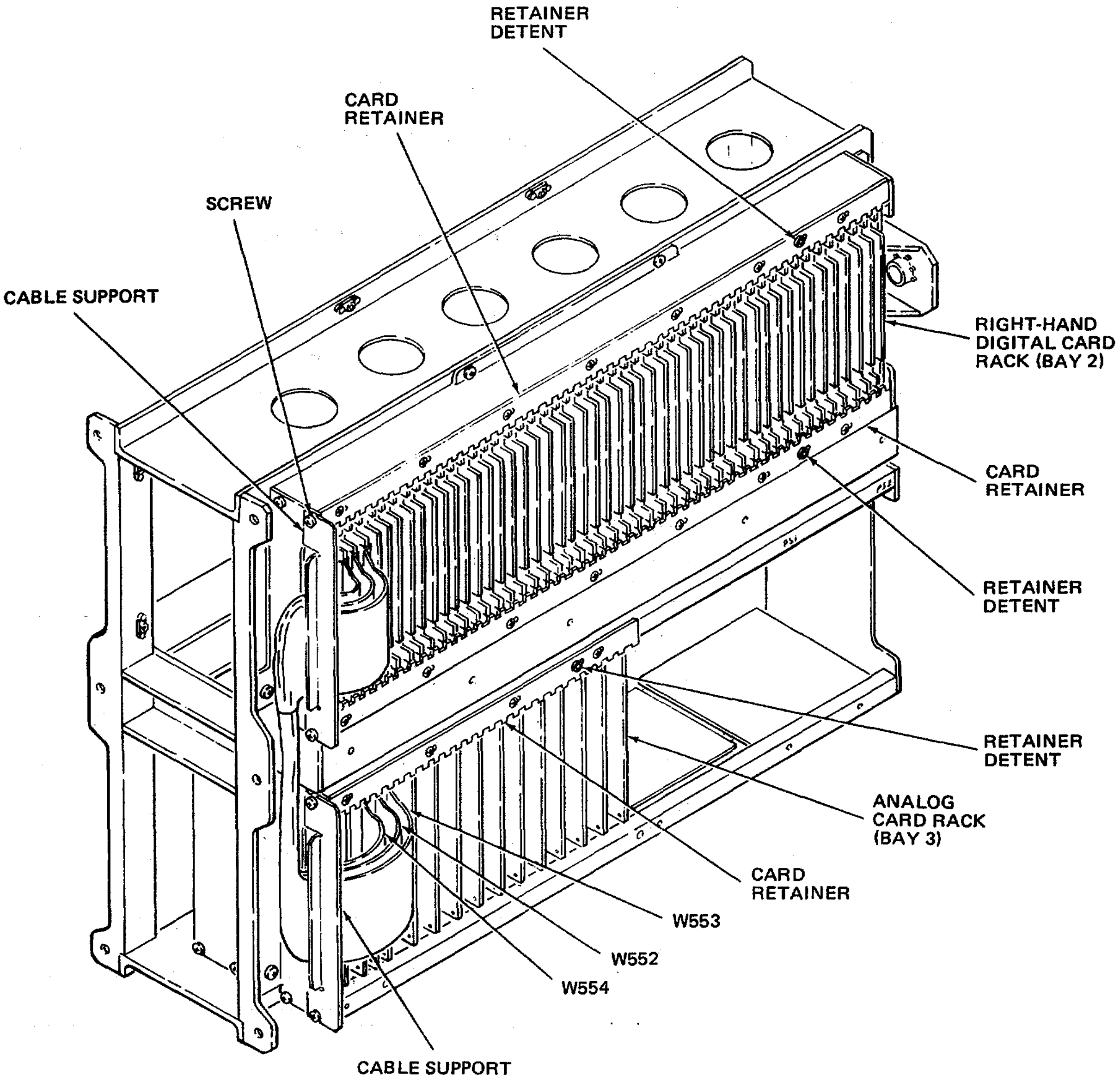
(2) Remove two screws securing each cable support to right-hand digital card rack (bay 2) and analog card rack (bay 3).

(3) Remove cable supports from card racks.

(4) Press retainer detent and slide card retainers to one side.

(5) Using card extractor, carefully remove cable assembly printed wiring boards from card racks.

(6) Remove cable assembly from MTS.



NOTE:
FRONT PANEL AND WIRING HARNESS REMOVED FOR CLARITY.

EL4QU024

Figure 3-8. Cable Assemblies W552, W553, and W554 Location

b. *Replacement.* Replace cable assembly as follows:

(1) Slide cable assembly printed wiring boards into card guides and insert in connector slot in card racks (refer to table 3-7).

(2) Slide card retainers back to original position until retainer detent locks.

(3) Carefully push loops of cable assemblies into recess between front panel and MTS frame as shown in figure 3-8.
(4) Place cable supports in position on end of card racks and secure each with two screws.

CAUTION

Ensure that the cable assemblies are properly tucked into the recess between the front panel and the frame to avoid damage when retracting the MTS into the case.

(5) Retract MTS into case following procedure of paragraph 3-11.

Table 3-6. Cable Assembly Installation

	From		To		
Reference designator	Bay	Slot	Bay	Slot	Part number
W552	2	03	3	02	10284102-6
W553	2	04	3	03	10284102-7
W554	2	05	3	01	10284102-8
W556	1	47	2	01	10284709-6

3-1 5. Cable Assembly W556 Removal and Replacement. Perform the following procedure to remove and replace cable assembly W556 (figure 3-9).

a. *Removal.* Remove cable assembly W556 as follows:

(1) Extend MTS from case following procedure of paragraph 3-11.

(2) Remove two screws securing cable support to right-hand digital card rack (bay 2).

(3) Remove cable support from right-hand digital card rack.

(4) Carefully push cable assemblies W552, W553, and W554 aside.

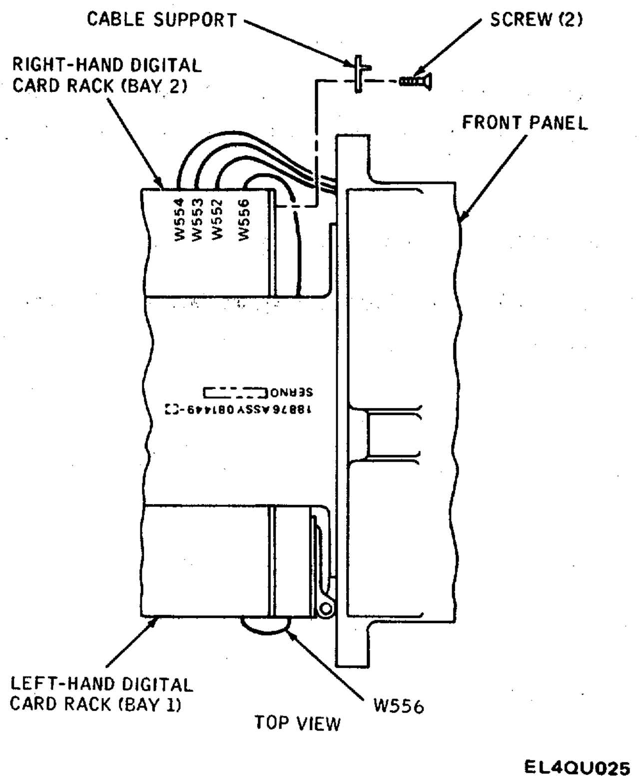


Figure 3-9. Cable Assembly W556 Location

(5) Press retainer detents on card retainers on both digital card racks (bays 1 and 2) and push to one side.

(6) Using card extractor, carefully remove cable assembly printed wiring boards from digital card racks.

(7) Remove cable assembly W556 from MTS.

b. *Replacement*. Replace cable assembly W556 as follows:

(1) Slide cable assembly printed wiring boards into card guides and insert in connector slots in digital card racks (refer to table 3-7).

(2) Slide card retainers back to original position until retainer detent locks.

(3) Carefully push loops of cable assemblies W552, W553, and W554 into recess between front panel and frame assembly.

(4) Place cable support in position on end of right-hand digital card rack and secure with two screws.

CAUTION

Ensure that the cable assemblies are properly tucked into the recess between the front panel and the frame to avoid damage when retracting the MTS into the case.

(5) Retract MTS into case following procedure of paragraph 3-11.

3-16. Wired Plug-In Unit Test Assembly Removal and Replacement. Perform the following procedure to remove and replace the wired plug-in unit test assembly.

NOTE

The wired plug-in unit test assembly consists of the MTS minus the case, circuit cards, and dc/dc converters.

a. Removal Remove wired plug-in unit test assembly as follows:

(1) Extend MTS from case following procedure of paragraph 3-11.

(2) Remove circuit cards and dc/dc converters PS1 and PS2 following procedures in TM 11-7010-201-12.

WARNING

Two men are required to remove the wired plug-in unit test assembly from the case to prevent injury to personnel or damage to the equipment.

(3) Simultaneously release slide locks on both slide rails, and then remove wired plug-in unit test assembly from case.

b. Replacement Replace wired plug-in unit test assembly as follows:

WARNING

Two men are required to install the wired plug-in unit test assembly into the case to prevent injury to personnel or damage to the equipment.

(1) Extend slide rail assemblies from case.

(2) Carefully align wired plug-in unit test assembly slide rails with case slide rails.

(3) Slide wired plug-in unit test assembly into case until slide locks engage.

(4) Install circuit cards and dc/dc converters PS1 and PS2 following procedures in TM 11-7010-201-12.

(5) Retract MTS into case following procedure of paragraph 3-11.

3-1 7. Connector J1, J2, and J4 Contact Removal and Replacement. Perform the following procedures to remove and replace any of the contacts in front panel connectors J1, J2, or J4.

a. *Removal* Remove contact from connector J1, J2, or J4 as follows:

(1) Gain access to rear of MTS front panel following procedure in paragraph 3-12.

(2) Remove four screws securing connector to front panel (figure 3-10) and carefully remove wired connector from rear of front panel.

(3) Insert extraction tool (MS3344-23 or equivalent) into appropriate connector cavity from mating side of connector.

NOTE

While inserting the extraction tool, rotate the tool in a circular pattern.

(4) Remove contact and attached wire from cable side of connector.

(5) To disconnect contact from its wire, cut wire as close to contact as possible.

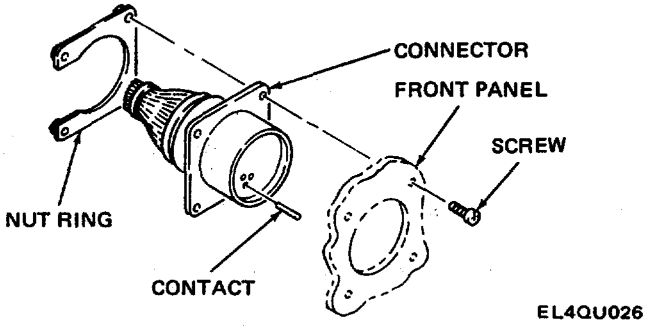


Figure 3-10. Front Panel Connector Removal

b. *Replacement*. Replace contact in connector J1, J2, or J4 as follows:

(1) Strip just enough insulation from wire to allow it to bottom out in barrel of contact.

(2) Insert wire into contact until it bottoms out; stripped wire should be visible through contact inspection hole, and wire insulation should butt against contact.

(3) Using crimp tool (M2252012-01 or equivalent) and positioner (M22520/2-03 or equivalent), insert contact and wire into well of crimp tool.

(4) To crimp contact and wire, squeeze handles of crimp tool until completely closed.

(5) Using insertion tool (MS3323-22 or equivalent), insert contact and wire into appropriate connector cavity from wiring side of connector.

NOTE

Ensure that contact is fully seated in connector.

(6) Install connector into front panel; secure with four screws and nut ring (figure 3-10).

(7) Secure front panel of MTS to chassis following procedure in paragraph 3-12.

3-18. Connector J3 Contact Removal and Replacement. Perform the following procedures to remove and replace any of the contacts in front panel connector J3.

a. *RemovaL Remove contact from connector J3 as follows*:

(1) Gain access to rear of MTS front panel following procedure in paragraph 3-12.

(2) Remove four screws securing connector to front panel (figure 3-10) and carefully remove wired connector from rear of front panel.

(3) Insert extraction tool (NAS1664-20 or equivalent) into appropriate connector cavity from mating side of connector.

NOTE

While inserting the extraction tool, rotate the tool in a circular pattern.

(4) Remove contact and attached wire from cable side of connector.

(5) To disconnect contact from its wire, Cut wire as close to contact as possible.

b. *Replacement Replace contact in connector J3 as follows:*

(1) Strip just enough insulation from wire to allow it to bottom out in barrel of contact.

(2) Insert wire into contact until it bottoms4,out; stripped wire should be visible through contact inspection hole, and wire insulation should butt against contact.

(3) Using crimp tool (M22520/1-01 or equivalent) and positioner (M22520/1-02 or equivalent), insert contact and wire into well of crimp tool.

(4) To crimp contact and wire, squeeze handles of crimp tool until completely closed.

(5) Using insertion tool (NAS1664-20 or equivalent), insert contact and wire into appropriate connector cavity from wiring side of connector.

NOTE

Ensure that contact is fully seated in connector.

(6) Install connector into front panel; secure with four screws and nut ring (figure 3-10).

(7) Secure front panel of MTS to chassis following procedure in paragraph 3-12.

3-19. Connector J7 Contact Removal and Replacement. Perform the following procedures to remove and replace any of the contacts in front panel connector J7.

a. *RemovaL Remove contact from connector J7 as follows:*

(1) Gain access to rear of MTS front panel following procedure in paragraph 3-12.

(2) Insert extraction tool (Winchester 107-1012 or equivalent) into appropriate connector cavity from mating side of connector.

NOTE

While inserting the extraction tool, rotate the tool in a circular pattern.

(3) Remove contact and attached wire from cable side of connector.

(4) To disconnect contact from its wire, cut wire as close to contact as possible.

b. *Replacement Replace contact in connector J7 as follows:*

(1) Strip just enough insulation from wire to allow it to bottom out in barrel of contact.

(2) Insert wire into contact until it bottoms out; stripped wire should be visible through contact inspection hole, and wire insulation should butt against contact.

(3) Using crimp tool (Winchester 107-0610 or equivalent) and positioner (Winchester 107-0603 or equivalent), insert contact and wire into well of crimp tool.

(4) To crimp contact and wire, squeeze handles of crimp tool until completely closed.

(5) Using insertion tool (Winchester 107-1011 or equivalent), insert contact and wire into appropriate connector cavity from wiring side of connector.

NOTE

Ensure that contact is fully seated in connector.

(6) Secure front panel of MTS to chassis following procedure in paragraph 3-12.

3-20. Card Rack Repair. General Support maintenance personnel are authorized limited wire-wrap repair of the digital and analog card racks. (Card rack removal and replacement is performed at the depot level.) Refer to table 3-6 to select the appropriate wire list. General card rack repair procedures are described in the following paragraphs.

a. *Digital Card Rack Access.* Perform the following procedure to gain access to the rear of the digital card racks (figure 3-11).

(1) Release four captive screws securing left-hand card rack to frame.

(2) Swing left-hand digital card rack away from rear of frame.

(3) To secure left-hand digital card rack, close rack and secure to frame using four captive screws.

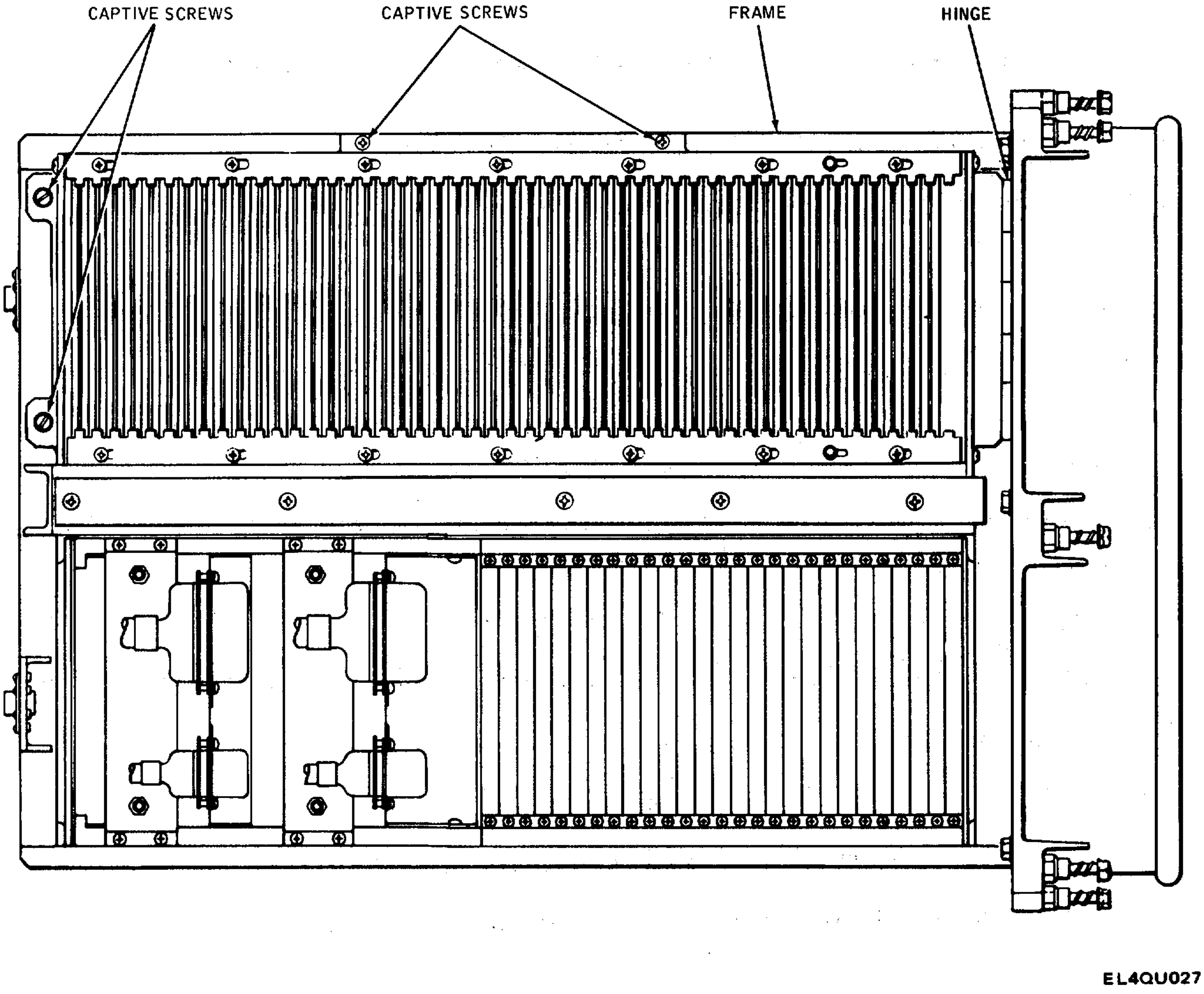


Figure 3-11. Card Rack Access

b. *Wire- Wrap Post Acces8.* Some wire-wrap posts are covered by connectors from the wiring harness. To gain access to these wire-wrap posts, see figure 3-12 and perform the following procedure.

(1) Remove connector from wire-wrap posts as follows:

(a) Remove two screws securing connector to card rack.

CAUTION

Use extreme care when removing connector. Do not use large screwdrivers or pliers, or the connector may break. Use a small, 90-degree offset screwdriver, hex wrench, or similar tool to gently pry up each end of the connector a little at a time.

(b) Remove connector from card rack.

(2) Replace connector as follows:

(a) Carefully install connector over wire-wrap posts on card rack.

(b) Apply liquid locking sealant (MIL-S-22473, Grade C) to screw threads.

(c) Secure connector to card rack using two screws.

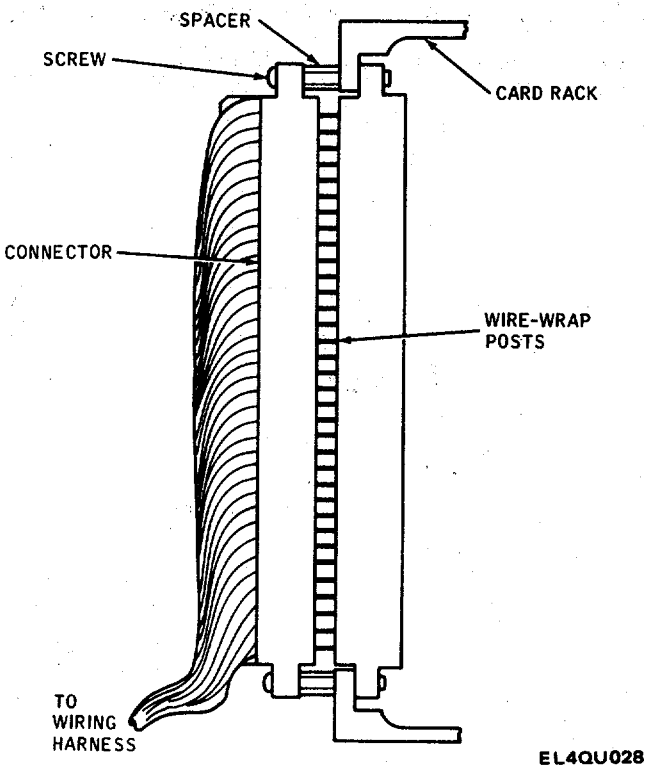


Figure 3-12. Wire-Wrap Post Access

c. *Wiring Repair Using Jumper Clips*. Use the following procedure for temporary repair of a broken wire-wrapped wire. Since this repair is only temporary, a new wire must be installed using the wire-wrap technique (paragraph e below) at the earliest opportunity.

CAUTION

Exercise care when working around wire-wrap post to prevent damage to wiring and other wire-wrap posts.

(1) Clip ends of broken wire as close to wire-wrap post as possible.

(2) When possible, remove broken wire from wire bundle. If removal is not practical, clip off ends of broken wire to prevent contact with other connections and leave broken wire in bundle.

(3) Unwrap broken wire fragments from wire-wrap posts.

(4) Measure distance between two points to be connected and cut a piece of 30 AWG insulated wire approximately one inch longer than distance measured.

(5) Strip insulation back 1/4-inch from each end of wire.

(6) Cut two 3/16-inch pieces of electrical heat-shrinkable insulation sleeving (Military Specification MIL-I-22129) and slip sleeving over ends of wire and push up out of way.

(7) Place end of wire (see figure 3-13) between flat tab and body of jumper clip (Berg Electronics part no. 47539 or equivalent) and bend tab against body.

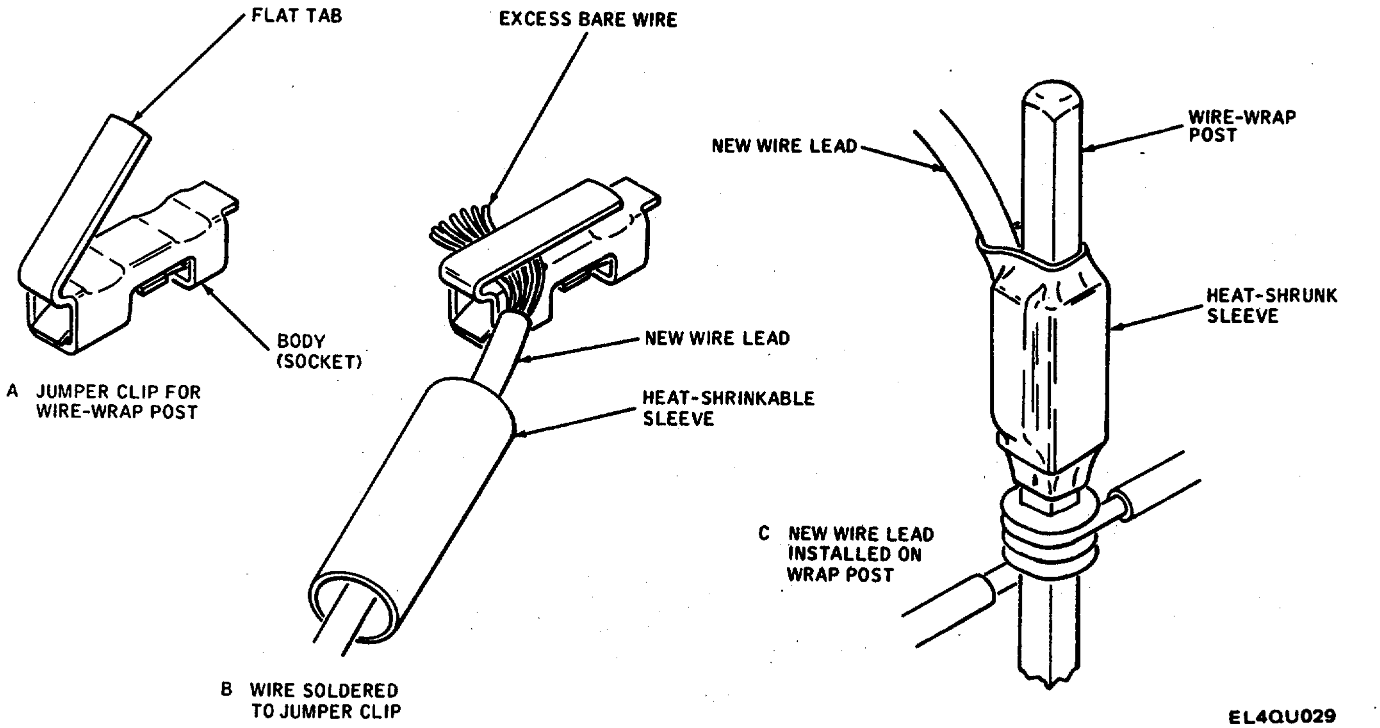


Figure 3-13. Wiring Repair Using Jumper Clips

(8) Heat end of wire with soldering iron, and apply solder to wire; solder should flow smoothly under tab.

(9) When solder has cooled, clip off excess bare wire.

(10) Repeat steps (7) thru (9) for other end of wire.

(11) Bend wire back along body of jumper clip.

(12) Slide heat-shrinkable insulation sleeving over jumper clip and heat sleeving lightly by bringing soldering iron close to sleeving until shrinkage stops.

(13) Install replacement wire by pushing each jumper clip down on wire-wrap posts.

(14) Carefully clean reworked area and reassemble MTS.

d. *Pyramiding Wire Replacement* . When new wiring must be installed, the degree of pyramiding must fit be determined before proceeding. The general restrictions are:

(1) A wire that has been unwrapped cannot be rewrapped. If an adequate service loop is available, the wire can be clipped and rewrapped; if not, a new wire must be installed.

(2) No more than three wires can be wrapped on a single pin; a wire that has been clipped off and left in place counts as one of the three.

(3) Unwrapping a clipped wire and sliding the topmost wire(s)-down is not permissible.

An example is provided where a wire must be replaced as shown in figure 3-14, example A. Wires A and B must be removed to remove wire C from pin 1. Figure 3-14, example B, shows the wires removed; and figure 3-14, example C, shows the new wires (AA and AC) installed, with the exception of wire AB to pin 4. Since three connections are already in place (X, Y, and B cut-end), these three connections must be removed to permit wrapping wire AB. However, if wires X and Y were to be replaced, a pyramiding condition could been countered where it may become impractical and too time-consuming to replace all other affected wires; i.e., all other wires related to wires X and Y replacement. A judgment is then necessary before starting to replace any wire, whether card cage repair or replacement should be undertaken.

e. *Wire-Wrap Repair*. Use the following procedure for permanent repair of broken wire-wrapped wire.

(1) Carefully strip insulation from each end of wire to length shown below.

(a) Strip 26 AWG wire 718 inch.

(b) Strip 30 AWG wire 1 inch.

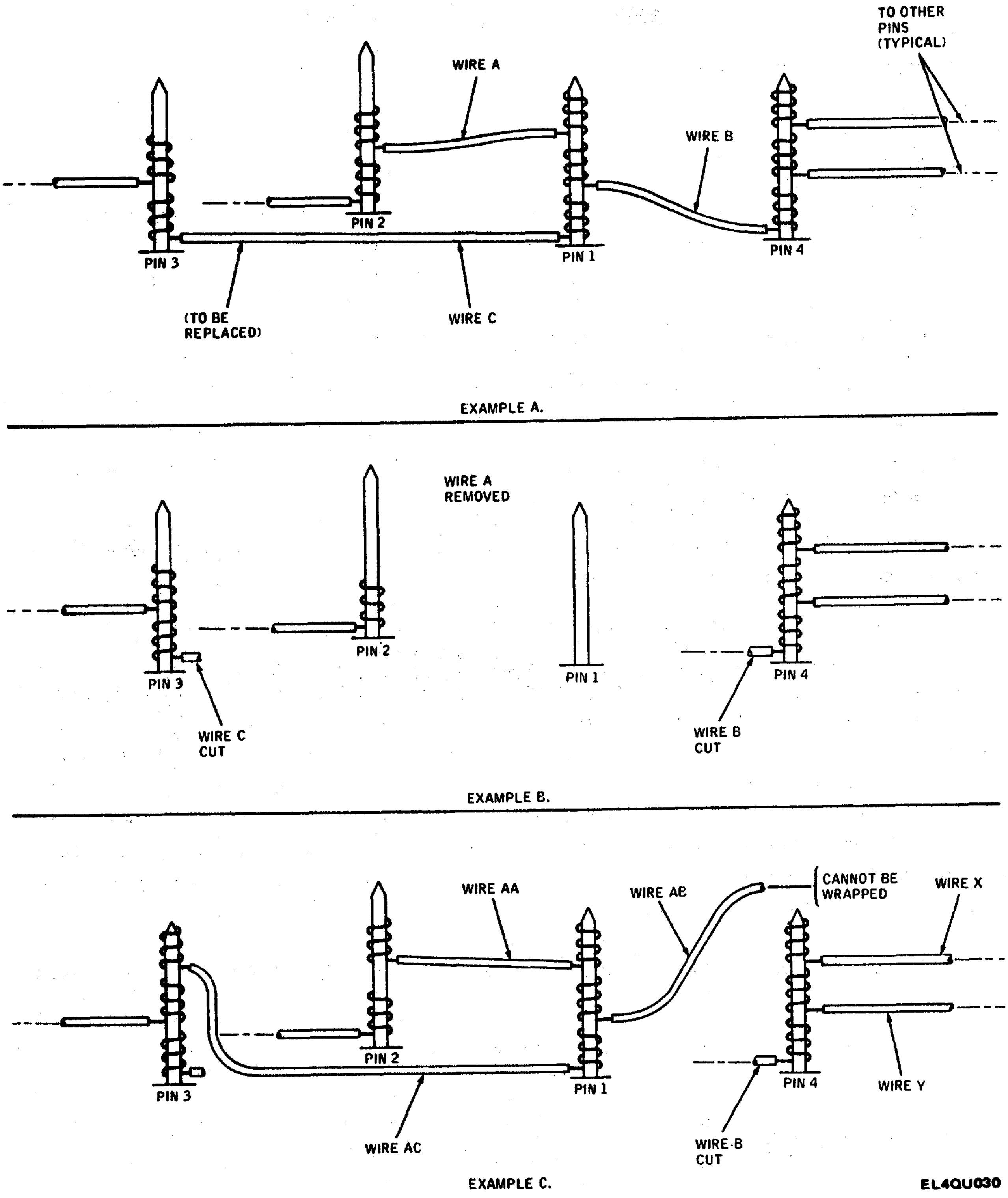


Figure 3-14. Pyramiding Wire Replacement Example

(2) Inspect stripped wire ends for nicks or cuts; neither are acceptable.

NOTE

The following general notes apply to all wire-wrap procedures:

A minimum 1/2 turn of insulated wire shall be wrapped around the wire-wrap post.

That portion of a wrap termination that has been removed or unwrapped shall not be used again. If there is sufficient unused wire, as from service loops, the wire may be re-stripped and a new wrap termination made. If not, replace the wire.

If it is impossible to remove a wire from a wire-wrap post, it is acceptable to cut the wire at the wire-wrap post. The clipped end shall not protrude more than 1/ 32-inch.

DO NOT relocate or reposition a wrap. If movement is necessary, cut off old and make a new wire-wrap.

(3) Select proper bit and sleeve from tool kit.

(4) Position lead to be wrapped so that subsequent routing of wire will not tend to unwrap connection.

(5) Insert stripped wire end into wrapping bit feed slot and anchor lead as shown in figure 3-15.

NOTE

Insert the insulated portion of the wire from 1/16 to 1/8 inch into the wrapping bit feed slot.

(6) Place wire-wrap tool over wire-wrap post.

(7) Holding tool perpendicular to connector, make wire-wrap as follows:

(a) When using power wire-wrap gun, press trigger and allow tool to complete wrap.

NOTE

Do not apply hand pressure to assist the tool.

(b) When using hand wire-wrap tools, apply continuous twisting motion to complete wrap.

NOTE

Do not press down on the tool while twisting.

(c) Remove tool from wire-wrap post.

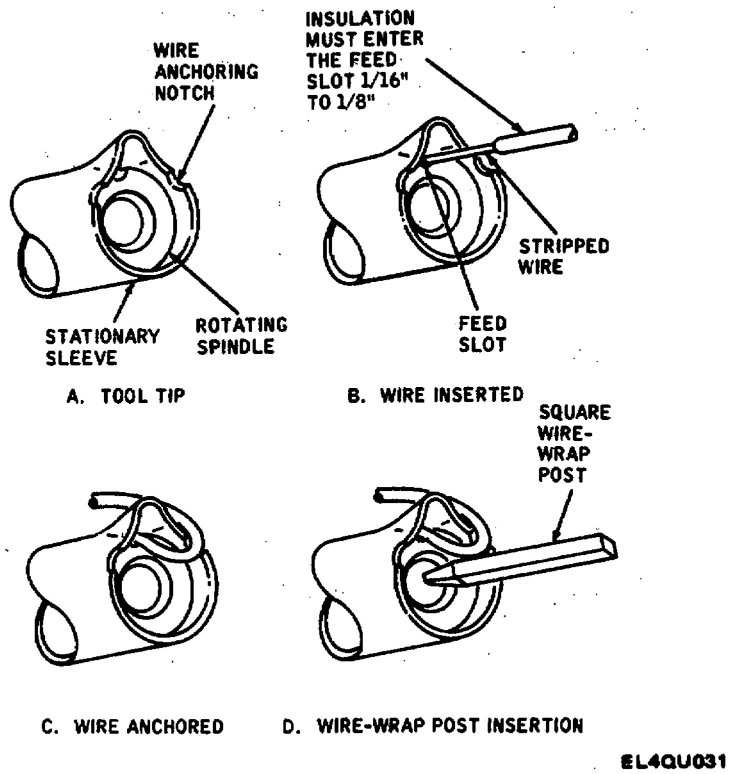


Figure 3-15. Wire-Wrap Connection Process

3-21. AC and DC Power Cable Repair. The ac and dc power cable repair consists of removing and replacing solder contact connectors. The ac power cable contains a molded plug on one end which is non-repairable. Perform the following procedure to remove and replace cable connector.

a. *Removal.* Remove cable connector as follows:

(1) Loosen two screws securing strain relief clamp, and slide strain relief clamp with grommet seal away from connector.

(2) Tag and unsolder connector wires.

b. *Replacement.* Replace cable connector as follows:

(1) Clean off excessive solder from wire, and insert into contact until it bottoms out.

(2) Solder wire to connector pin.

(3) Slide strain relief clamp with grommet seal on connector, and tighten two screws.

Section V. GENERAL SUPPORT TEST PROCEDURES

3-22. Introduction. This section provides test procedures authorized for General Support maintenance of the MTS. Cable assemblies are tested after removal from the MTS following the applicable procedure in section IV. The wired plug-in unit test assembly is tested as part of the MTS. The self-test procedure for the MTS (TM 11-7010-201-12) is to be performed after completion of any of the maintenance procedures in this manual. Satisfactory completion of the self-test procedure verifies that the MTS is in serviceable condition.

3-23. Cable Assemblies W552, W553, W554 and W556 Test Procedure. Testing of cable assemblies W552, W553, W554 and W556 consists of continuity (resistance) measurements from terminal to terminal and wire to wire. Perform the following procedure to test a cable assembly.

a. Set up multimeter for resistance checks.

NOTE

All cable wiring is pin to pin; for example: pin 1 of P1 to pin 1 of P2, pin 2 of P1 to pin 2 of P2, etc.

b. Measure resistance from P1 pin 1 to P2 pin 1, P1 pin 2 to P2 pin 2, etc., until all 80 pins are checked. Multimeter shall indicate short circuit for each measurement.

c. Measure resistance from P1 (or P2) pin 1 to P1 (or P2) pin 2, P1 (or P2) pin 2 to P1 (or P2) pin 3, etc., until all adjacent pins are checked. Multimeter shall indicate open circuit for all measurements.

d. Replace cable assembly if either test b or test c is failed.

3-24. Wire Plug-In Unit Test Assembly Test Procedure. The wired plug-in unit test assembly is tested as part of the complete MTS. Perform the following procedure to test the wired plug-in unit test assembly.

a. Perform MTS self-test procedure in TM 11-7010-201-12.

b. If self-test procedure indicates fault, perform MTS fault isolation procedure in TM 11-7010-201-12.

NOTE

An oscilloscope may be used for making voltage measurements specified in the fault isolation procedure, which calls for a multimeter.

c. If test fails, replace wired plug-in unit test assembly following procedure described in paragraph 3-16.

APPENDIX A

REFERENCES

DA PAM 310-1	Consolidated Index of Army Publications and Blank Forms
SB 11-573	Painting and Preservation Supplies Available for Field Use for Electronics Command Equipment
TM 11-5805-681-12	Operator's and Organizational Maintenance Manual, Automatic Telephone Central Office AN/TTC-39 (V) (NSN 5805-01-122-3414) (NSN 5805-01-121-4395) (NSN 5805-01-121-9560)
TM 11-5805-683-12 EE119-AA-OMI-010/E154 TYC39 T.O. 31W2-2TYC-39-11	Operator's and Organizational Maintenance Manual, Automatic Message Switching Central AN/TYC-39 (V) (NSN 5805-01-123-1851)
TM 11-6625-654-14	Operator's Organizational, Direct Support, and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools List) for Multimeter AN/USM-223 (NSN
TM 11-6625-2735-14 0969-LP-170-1090 T.O. 33Al-13-498-1	Operator's, Organizational, Direct Support, and General Support Maintenance Manual (Including Depot Maintenance) for Oscilloscope OS-261/U (NSN 6625-00-127-0079)
TM 11-7010-201-12 ET821-AA-OMI-O0I/E154 MTS T.O. 033-1078)	Operator and Organizational Maintenance Manual, Test Set, Electronic Circuit Plug-In Unit TS-3317 ( )/TSQ-73 (NSN 1430-01-
TM 11-7010-201-40P ET821-AA-PLG-010/E154 MTS T.O. 31S5-2TSQ73-4	Organizational and General Support Maintenance Repair Parts and Special Tools List (Including Depot Maintenance Repair Parts and Special Tools) for Test Set, Electronic Circuit Plug-In Unit TS-3317 ( )/TSQ-73 (NSN 1430-01-033-1078)
TM 38-750	The Army Maintenance Management System (TAMMS)
TM 740-90-1	Administrative Storage of Equipment
TM 746-10	Field Instructions for Painting and Preserving Electronics Command
TM 750-244-2	Procedures for Destruction of Electronics Materiel to Prevent Enemy Use (Electronics Command)

APPENDIX B

EXPENDABLE SUPPLIES AND MATERIALS LIST

Section I. INTRODUCTION

B-1. Scope

This appendix lists expendable supplies and materials you will need to operate and maintain the TS-3,317( )/TSQ-73. These items are authorized to you by CTA 50-970, Expendable Items (Except Medical, Class V, Repair Parts, and Heraldic Items).

B-2. Explanation of Columns

a. Column 1 - Item Number. This number is assigned to the entry in the listing and is referenced in the narrative instructions to identify the material (e.g., "Use cleaning compound, item 5, App. D").

b. Column 2 - Level. This column identifies the lowest level of maintenance that requires the listed item.

C - Operator/Crew
O - Organizational Maintenance
F - Direct Support Maintenance
H - General Support Maintenance

c. Column 3 - National Stock Number. This is the National stock number assigned to the item; use it to request or requisition the item.

d. Column 4 - Description. Indicates the Federal item name and, if required, a description to identify the item. The last line for each item indicates the part number followed by the Federal Supply Code for Manufacturer (FSCM) in parentheses, if applicable.

*e. Column 5 **-** Unit of Measure (U/M).* Indicates the measure used in performing the actual maintenance function. This measure is expressed by a two-character alphabetical abbreviation (e.g., ea, in, pr). If the unit of measure differs from the unit of issue, requisition the lowest unit of issue that will satisfy your requirements.

(1) Level	(2) National Stock Number	(3) Description	(4) U/M
H	7920-00-924-5700	Cloth, Cleaning	EA
H	6850-00-105-3084	Trichlorotrifluoroethane	16 oz

GLOSSARY

A

ADRS	address
ASSY	assembly

B

B	before

C

CB	circuit breaker
CHG	change
CHK	check
CMPNT	component
CONDTN	condition
CONN	connect, connector
CONV	converter
CTR	counter
CUT	card under test

D

D	during
DC	direct current
DIV	divide
DS/GS	direct support/general support

E

EIR	equipment improvement recommendations
EXT	external, extinguish

F

FI	fault isolation

G

GEN	generator

I

I	intermediate
IC	integrated circuit
ID	identification
IND	indicator, indication
INDV	individual
INT	internal
I/O	input/output
LOC	input/output controller
IROAN	inspect and repair only as necessary

L

LED	light emitting diode
LSB	least significant bit
LT	light

M

MAC	maintenance allocation chart
MAG	magnetic
MSB	most significant bit
MSEC	millisecond
MTS	module test set
MWO	modification work order

N

NO	number
NSN	national stock number

O

ORIG	original

P

PC	printed circuit
PMCS	preventive maintenance checks and services
PROM	programmable read-only memory
PWR	power

R

RECONN	reconnect
REF	reference

S

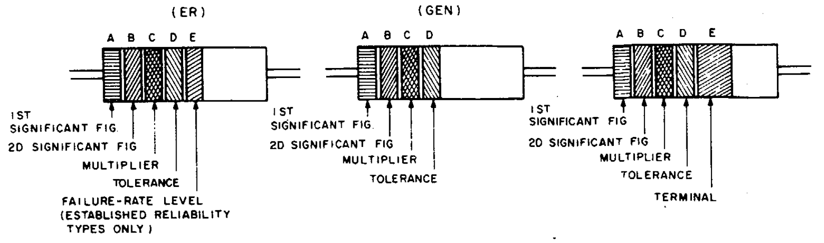
SEC	second
SPLY	supply
SW	switch

U

U/P	unused pin
UUT	unit under test

V

V	volt
VDC	volt, direct current



COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY).			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS) ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL

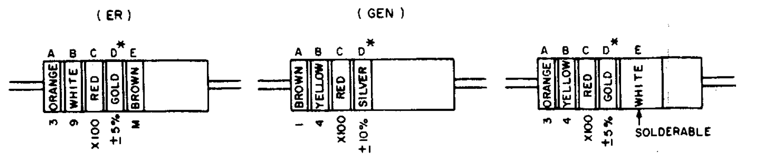
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS
(THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHM ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS   10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 3,900 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

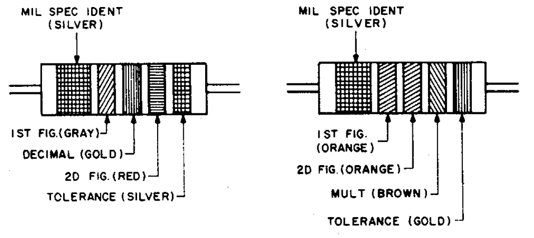
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



(A) 8.2UH ± 10%   (B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 8.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330 UH INDUCTOR ARE ILLUSTRATED.

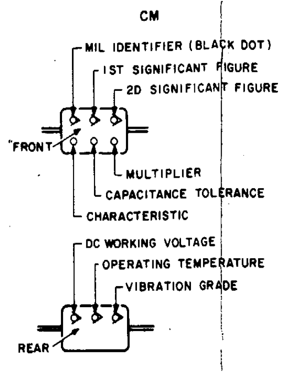
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

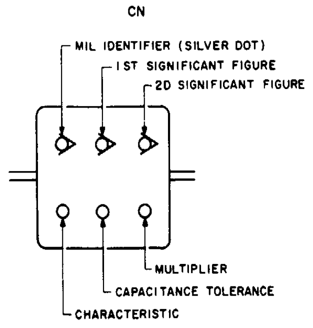
MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

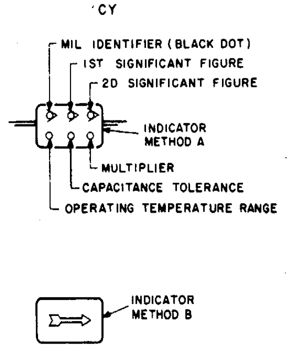
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.



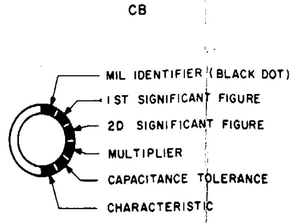
MICA-DIELECTRIC



PAPER-DIELECTRIC



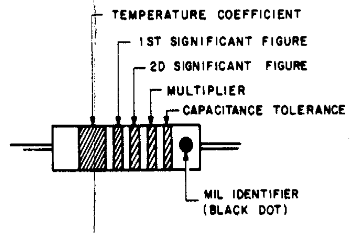
GLASS-DIELECTRIC, GLASS CASE



MICA, BUTTON TYPE

TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CM	CY, CM	CM
BLACK	CM, CY CB	0	0	1			±20%	±20%		A			-55° TO +70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55° TO +85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55° TO +125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55° TO +150°C	
PURPLE (VIOLET)		7	7											
GRAY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN			0.01	±10%	±10%	±10%	±10%						



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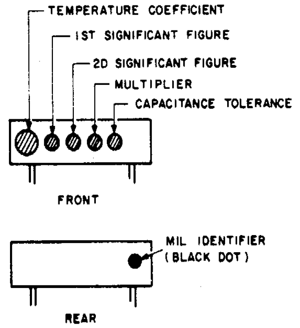
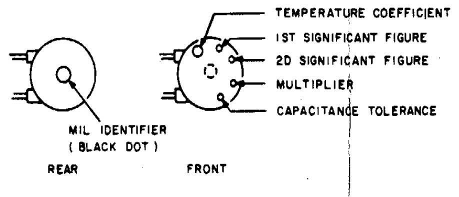


RADIAL LEAD



DISK-TYPE

TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GRAY		8	8	0.01*			
WHITE		9	9	0.1*	±10%		
GOLD	+100			0.1		±1.0 UUF	
SILVER				0.01			

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-25D, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

* OPTIONAL CODING WHERE METALLIC PIGMENTS ARE UNDESIRABLE.

EL4QU034

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

Figure FO-1. Standard Color Coding Chart

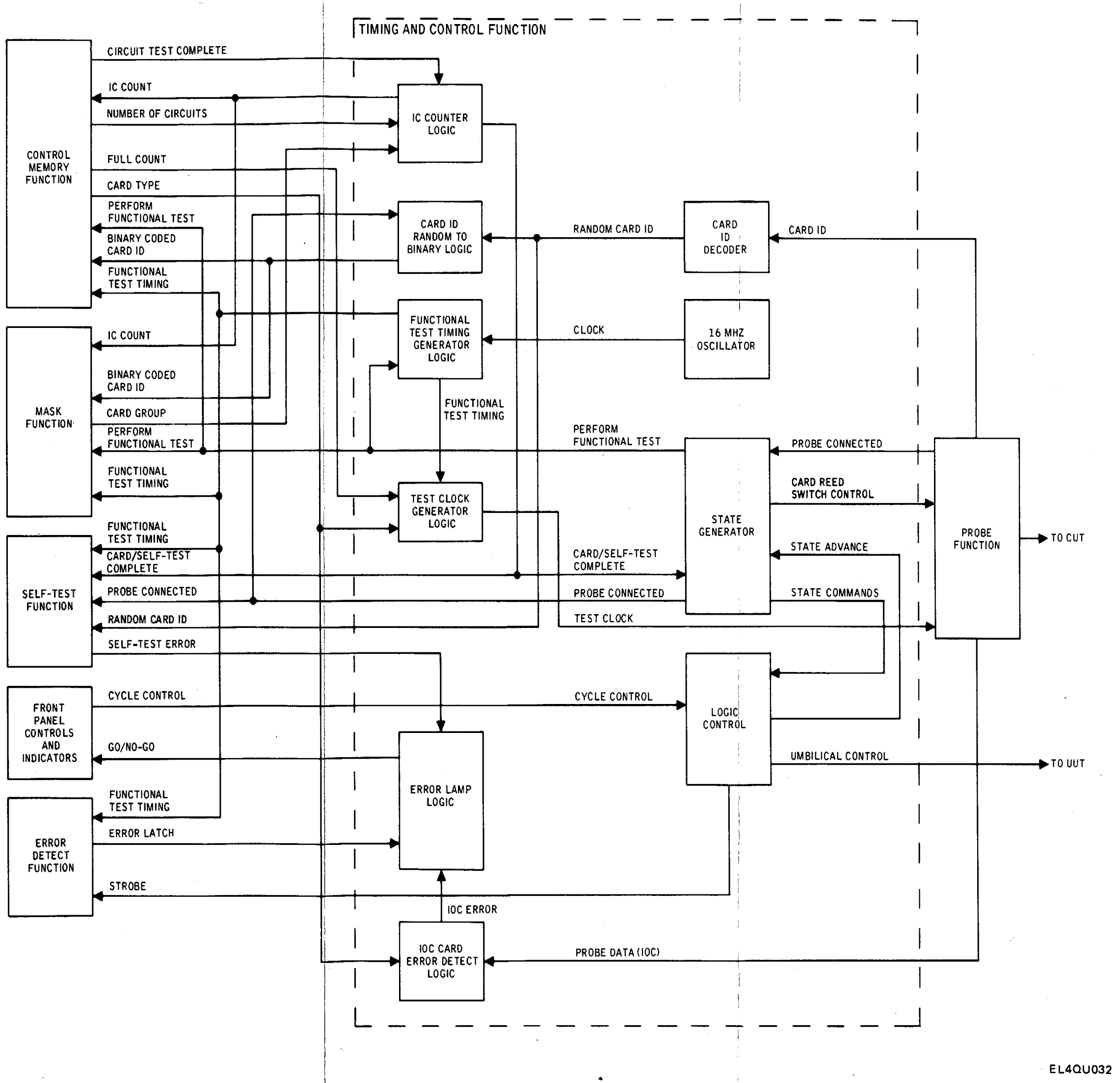
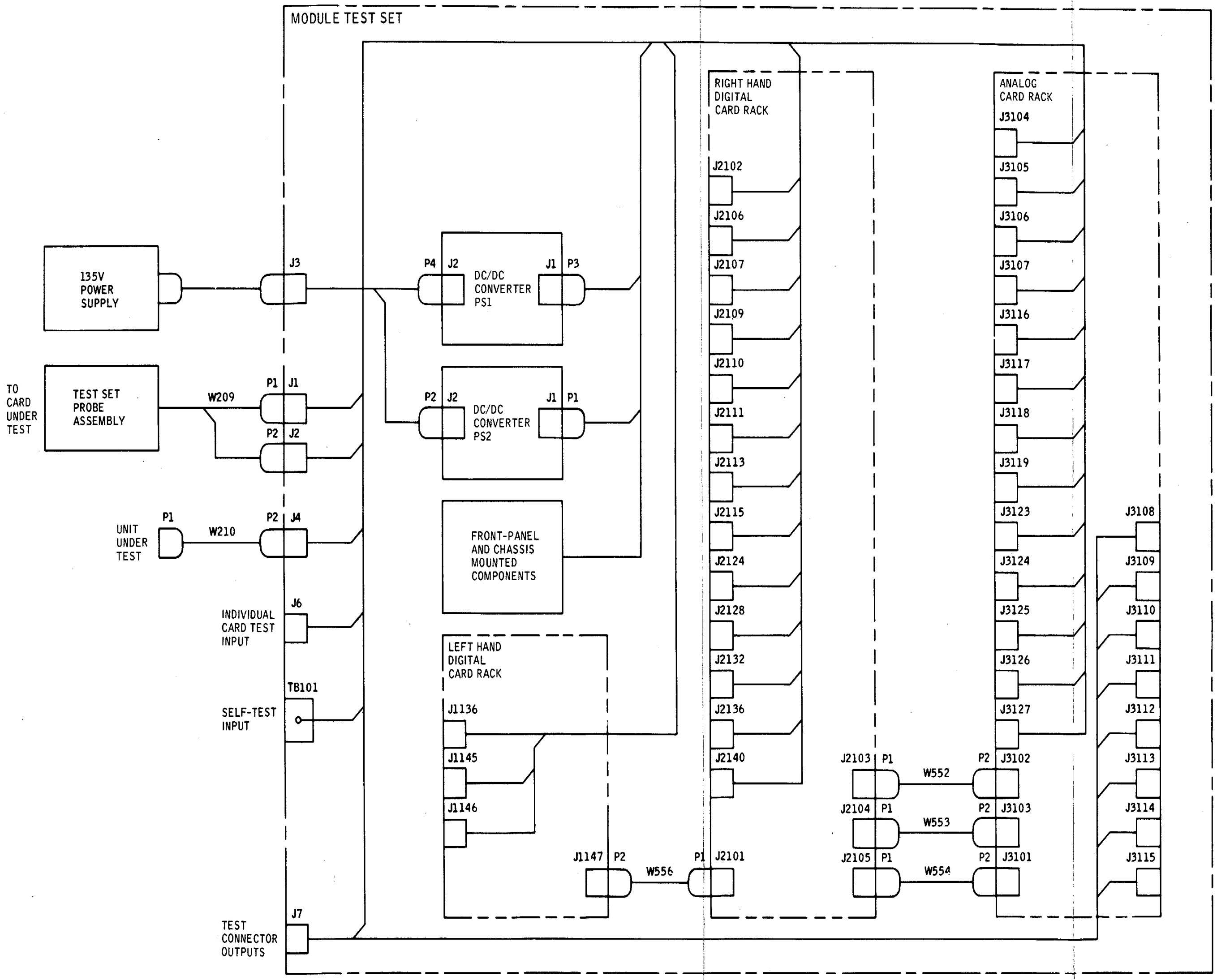


Figure FO-2. Timing and Control Function

Figure FO-2. Timing and Control Function Block Diagram



NOTES:

1. TEST SET PROBE ASSEMBLY 135V POWER SUPPLY AND EXTERNAL CABLES SHOWN FOR REFERENCE ONLY.
2. INTERNAL WIRE HARNESS INTERCONNECTIONS ARE THROUGH REAR CONNECTORS ATTACHED TO CARD CONNECTOR WIRE-WRAP PINS.

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Figure FO-3. MODULE Test Set Cabling Diagram

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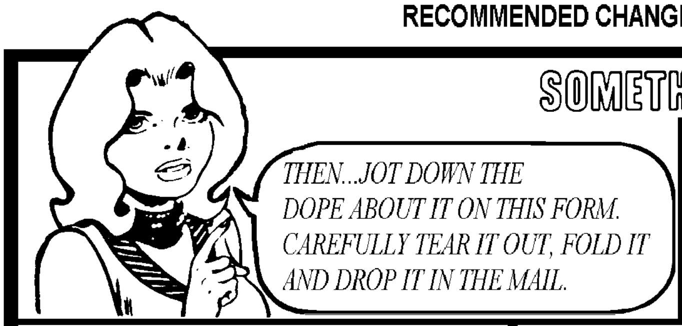

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